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Two types of high-temperature superconducting (HTS) multichip modules (MCMs), utilizing yttrium-barium-copper oxide (YBCO) as the superconductor, were developed under this grant. The first was a "flip mesh" MCM, in which two superconducting layers, one containing X-running and one Y-running wire segments, were fabricated on separate substrates and joined in a manner similar to flip chips.

The second module was a monolithic MCM, again using layers of X- and Y-running conductors, but patterned on a single substrate, with a thick layer of SiO_2 serving as interlayer dielectric. Deposition of the second superconducting (YBCO) layer was effected by the use of an ion beam-assisted deposition (IBAD) buffer layer.

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ABSTRACT

Two types of high-temperature superconducting (HTS) multichip modules (MCMs), utilizing yttrium-barium-copper oxide (YBCO) as the superconductor, were developed under this grant. The first was a "flip mesh" MCM, in which two superconducting layers, one containing X-running and one Y-running wire segments, were fabricated on separate substrates and joined in a manner similar to flip chips.

The second module was a monolithic MCM, again using layers of X- and Y-running conductors, but patterned on a single substrate, with a thick layer of SiO_2 serving as interlayer dielectric. Deposition of the second superconducting (YBCO) layer was effected by the use of an ion beam-assisted deposition (IBAD) buffer layer.

RESULTS

A great deal of progress was made toward realizing the flip-mesh MCM and the monolithic MCM, although neither were totally successful. Rather than repeat previously published material, the reader is referred to the enclosed papers presented at the May 1997 Electrochemical Society meeting. Presentation [11](principle author Cooksey, funded under this grant) describes the monolithic MCM, and presentation [12] (principal author Scott, funded under this grant) describes the "flip-mesh".

Although the final goal of reliably producing superconducting MCMs proved illusive, a great deal was learned about two important aspects of the creation of complex thin-film HTS structures: the deposition of superconducting layers over thick amorphous dielectric layers, and the process of creating vias between superconducting layers. These results, which go a long way in solving the most difficult problems associated with HTS multilayer structures, are discussed in Publications [11], [12], and [13].

The via structure described in [11], though made of normal metal (gold), represents a significant advance over previously reported superconducting vias, because it occupies relatively little space in an MCM structure, and contributes very little resistance compared with the resistance of normal metal lines. It is the line, not the via, resistance which was the impetus for HTS MCMs, in the first place.

The HTS layers described in [12] and [13], which use IBAD yttria-stabilized zirconia (YSZ) buffer layers to allow the deposition of an upper HTS layer over a thick SiO_2 interlayer dielectric, are a significant advance over previously reported HTS MCM work, which attempted to maintain multilayer epitaxy. The latter, maintenance of

multilayer epitaxy, resulted in an extremely thin, high dielectric constant interlayer dielectric, which would make the fabrication of transmission lines of usable impedance (~50-75 Ω) and reasonable propagation delay (<100 pS/cm) impossible. However, the fabrication of reasonable transmission lines is possible in the structures which have been developed under this grant. A monolithic HTS MCM was produced which appeared to superconduct and function as anticipated, before ultimately failing. The student responsible left for a job in industry before a second module was fabricated and these tantalizing results verified. New personnel, under another grant, are working to replicate the MCM.

CONCLUSION

Significant progress was made on two impediments to the realization of HTS MCMs. First, HTS YBCO was deposited and patterned atop a thick, amorphous dielectric (SiO_2). Second, functional gold vias between superconducting layers were developed. A multilayer HTS MCM was produced that appeared to function before its untimely failure. A complete set of the publications and presentations produced under this grant is included with this report.

PUBLICATIONS and PROCEEDINGS

[1] J. W. COOKSEY, W. D. BROWN, S. S. ANG, H. A. NASEEM, R. K. ULRICH, AND L. WEST, "Gamma-ray and fast neutron radiation effects on thin film superconductors," *IEEE Trans. Nucl. Sci.*, vol. 41, pp. 2521-2524, 1994.

[2] D. E. FORD, S. S. SCOTT, S. S. ANG, AND W. D. BROWN, "A comparison of high-temperature superconductors in multichip module applications," *Proc. Ark. Acad. Sci.*, vol. 48, pp. 45-49, 1994.

[3] R. G. FLORENCE, S. S. ANG, AND W. D. BROWN, "The effects of rapid thermal annealing on the properties of sputtered YBCO superconducting films," *Supercond. Sci. Technol.*, vol. 7, pp. 741-744, 1994.

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[5] G. FLORENCE, S. ANG, AND W. D. BROWN, "Ion beam assisted sputter deposition of CeO_2 buffer layers for superconducting multichip module (MCM) applications," *Electrochem. Soc. Proc.*, vol. 95-9, *Proceedings of the Symposium on Low Temperature Electronics and High Temperature Superconductivity*, pp. 113-120, 1995.

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[9] Q. XIONG, S. AFONSO, F. T. CHAN, K. Y. CHEN, G. J. SALAMO, G. FLORENCE, J. COOKSEY, S. SCOTT, S. ANG, W. D. BROWN, AND L. SCHAPER, "Fabrication of highly textured superconducting thin films on polycrystalline substrates using ion beam assisted deposition," *Proceedings of the 10th Anniversary HTS Workshop on Physics, Materials and Applications*, B. BATLOGG, C. W. CHU, W. K. CHU, D. U. GUBSER, and K. A. MÜLLER eds. World Scientific: New Jersey 1996, pp. 167-170.

[10] J. W. COOKSEY, S. S. SCOTT, W. D. BROWN, S. S. ANG, R. G. FLORENCE, AND S. AFONSO, "Recent advances in high temperature superconductor multichip modules," *Proc. 1997 ICEMCM*, pp. 115-120, 1997.

[11] J. W. COOKSEY, S. AFONSO, W. D. BROWN, L. W. SCHAPER, S. S. ANG, R. K. ULRICH, G. J. SALAMO, AND F. T. CHAN, "Fabrication and characterization of vias for contacting $YBa_2Cu_3O_{7x}$ multilayers," *Physica C*, vol. 282-287, pp. 683-684, 1997.

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[13] S. AFONSO, K. Y. CHEN, Q. XIONG, Y. Q. TANG, G. J. SALAMO, F. T. CHAN, J. COOKSEY, S. SCOTT, Y. J. SHI, S. ANG, W. D. BROWN, AND L. W. SCHAPER, "$Y_1Ba_2Cu_3O_{7-x}$ multilayer structures with a thick SiO_2 interlayer for multichip modules," *J. Mater. Res.*, vol. 12, pp. 2947-2951, 1997.

PRESENTATIONS

[1] D. E. FORD, S. S. SCOTT, S. S. ANG, AND W. D. BROWN, "A comparison of high-temperature superconductors in multi-chip module applications," *78th Annual Meeting of the Arkansas Academy of Science*, April 8-9, 1994, Jonesboro, AR, 1994.

[2] J. W. COOKSEY, W. D. BROWN, S. S. ANG, H. A. NASEEM, R. K. ULRICH, AND L. WEST, "Gamma-ray and fast neutron radiation effects on thin film superconductors," *31st Annual International Nuclear and Space Radiation Effects Conference*, July 18-22, 1994, Tucson, AZ, 1994.

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[4] G. FLORENCE, S. ANG, AND W. D. BROWN, "Ion beam assisted sputter deposition of CeO_2 buffer layers for superconducting multichip module (MCM) applications," *Symposium on Low Temperature Electronics and High Temperature Superconductivity at the 187th Meeting of the Electrochemical Society*, May 21-26, 1995, Reno, NV, 1995.

[5] S. S. SCOTT, S. S. ANG, AND W. D. BROWN, "The effects of low-energy blanket ion milling on the properties of superconducting YBCO films," *Symposium on Low Temperature Electronics and High Temperature Superconductivity at the 187th Meeting of the Electrochemical Society*, May 21-26, 1995, Reno, NV, 1995.

[6] S. AFONSO, F. T. CHAN, K. Y. CHEN, G. J. SALAMO, Y. Q. TANG, R. C. WANG, X. L. XU, Q. XIONG, G. FLORENCE, S. SCOTT, S. ANG, W. D. BROWN, AND L. W. SCHAPER, "The magnetic field and temperature dependence of critical current densities in multilayer $YBa_2CuO_{4+\delta}$," *40th Annual Conference on Magnetism and Magnetic Materials*, November 6-9, 1995, Philadelphia, PA, 1995.

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[8] J. W. COOKSEY, S. AFONSO, W. D. BROWN, L. W. SCHAPER, S. S. ANG, R. K. ULRICH, G. J. SALAMO, AND F. T. CHAN, "Fabrication and characterization of vias for contacting $YBa_2Cu_3O_{7-x}$ multilayers," *5th International Conference on Materials and Mechanisms of Superconductivity and High-Temperature Superconductors, M²S-HTSC-V*, February 28 - March 4, 1997, Beijing, China, 1997.

[9] S. AFONSO, K. Y. CHEN, Q. XIONG, F. T. CHAN, G. J. SALAMO, J. W. COOKSEY, S. SCOTT, S. ANG, W. D. BROWN, AND L. W. SCHAPER, "Fabrication techniques and electrical properties of $YBa_2Cu_3O_{7-x}$ multilayers with rf sputtered amorphous SiO_2 interlayers," *5th International Conference on Materials and Mechanisms of Superconductivity and High-Temperature Superconductors, M²S-HTSC-V*, February 28 - March 4, 1997, Beijing, China, 1997.

[10] J. W. COOKSEY, S. S. SCOTT, W. D. BROWN, S. S. ANG, R. G. FLORENCE, AND S. AFONSO, "Recent advances in high temperature superconductor multichip modules," *6th International Conference on Multichip Modules, ICEMCM '97*, April 2-4, 1997, Denver, CO, 1997.

[11] J. W. COOKSEY, W. D. BROWN, L. W. SCHAPER, R. G. FLORENCE, S. S. SCOTT, AND S. AFONSO, "Fabrication and characterization of a high temperature superconducting multichip module," *Fourth Symposium on Low Temperature Electronics and High Temperature Superconductivity at the 191st Meeting of the Electrochemical Society*, May 4-9, 1997, Montreal, Canada, 1997.

[12] S. S. SCOTT, S. S. ANG, W. D. BROWN, L. W. SCHAPER, AND S. AFONSO, "The flip-mesh superconducting MCM," *191st Meeting of the Electrochemical Society*, May 4-9, 1997, Montréal, Québec, Canada, 1997.

Gamma-ray and Fast Neutron Radiation Effects on Thin Film Superconductors*

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Abstract

The gamma-ray and neutron radiation hardness of $YBa_2Cu_3O_{7-x}$, $Tl_2Ba_2CaCu_2O_{8+x}$, and $Tl_2Ba_2Ca_2Cu_3O_{10+x}$ superconducting thin films deposited by off-axis sputtering and laser-ablation deposition techniques on substrates of MgO and $LaAlO_3$ was investigated. The unbiased samples were irradiated with 662 keV gamma-rays up to a cumulative dose of 1.5 Mrad(Si) and with neutron fluences up to 1×10^{14} neutrons/cm^2.

It was determined through nondestructive critical temperature transition, T_c, and critical current density, J_c, measurements and x-ray diffraction analysis that the thin film superconductors were radiation hard up to moderate levels of neutrons and gamma-rays. It was also determined that extended exposure to moderately humid air degraded the critical current density of all the films.

I. Introduction

Space applications of multichip modules (MCMs) appear to be part of the driving force for their development. In the future, thin film superconductors (TFSCs) will potentially be used as interconnects for MCMs. As a result of this application of TFSCs, their response to a radiation environment is of great interest. In the past, studies of radiation effects on superconductor materials have been restricted to the bulk form [1-5], but if superconducting interconnects are to be used in future MCMs, the impact of exposure to gamma-rays and fast neutrons on the properties of TFSC materials must be examined. In addition to the effects of radiation on the superconductor material, the substrate material on which the superconductor is deposited, as well as the dielectric material used to separate the multiple levels of interconnects, must also be examined for sensitivity to radiation exposure.

*We would like to acknowledge the assistance of Tim Welty of the Southwest Radiation Calibration Center in the radiation experiments. We would also like to acknowledge Conductus, Inc. and Superconductor Technologies Inc. for their donation of superconductor samples. This research was funded by E-Systems, Inc. and the Advanced Research Projects Agency.

II. Experimental Procedures

In the work reported here, $YBa_2Cu_3O_{7-x}$ (YBCO), $Tl_2Ba_2CaCu_2O_{8+x}$ (Tl-2212), and $Tl_2Ba_2Ca_2Cu_3O_{10+x}$ (Tl-2223) thin films on substrates of MgO and $LaAlO_3$, some of the more common superconductor/substrate combinations, were subjected to both gamma-ray and neutron radiation in an electrically unbiased state. Although radiation without bias does not fully explore the impact on dielectric substrates, it does examine the impact on high temperature superconductors. The samples were deposited using laser-ablation and off-axis sputtering techniques, and were of varying quality and thickness in order to determine if their radiation hardness varied accordingly. The thin film thicknesses ranged from about 200 to 1000 nm.

The superconductors were characterized by their critical temperature transition, T_c, and critical current density, J_c, measured using a nondestructive inductance method as described by Claassen et al. [6]. This measurement technique involves placing a thin, multiturn copper coil next to the film surface and driving the coil with a low distortion audio-frequency sine-wave current. In turn, the driving current induces shielding currents in the film. The nonlinearity in the coil-film system increases abruptly when the induced current in the film reaches its critical level. A schematic of the measurement system used is shown in Figure 1. The resulting voltage across the coil is filtered by a passive twin-tee notch filter with a center frequency the same as the drive current frequency, 1 kHz, and analyzed by the lock-in amplifier for third harmonics. Either a single or double coil can be used. A single coil acts as "both the drive and pickup coil." We have used a single coil setup in our measurements since it functions as well as a two coil setup according to Claassen et al. The samples were measured down to liquid nitrogen temperature (77 K). This type of measurement was chosen over the four point contact method because the samples had to be measured after each irradiation. Any probe technique would destroy a large surface area of the film after each subsequent measurement since we were dealing with samples less than 1 cm^2. A Philips x-ray diffractometer was also used in an attempt to detect any atomic disorder in the superconductor films resulting from neutron bombardment.

The superconductor/substrate structures were irradiated with gamma-rays up to a cumulative dose of 1.5 Mrad(Si)

using a Cs-137 radioisotope emitting 662 keV gamma-rays at a dose rate of 24.2 krad(Si)/hr. The gamma-ray source was contained in a JL Shepherd Model 81-12A Irradiator. The neutron irradiations involved exposing the samples to cumulative fluences up to 1 x 10^{14} neutrons/cm^2 from a 0.68 Ci Cf-252 source which had an average neutron flux throughout the experiment of 1.966 x 10^8 neutrons/cm^2·s. All irradiations were performed in air at room temperature.

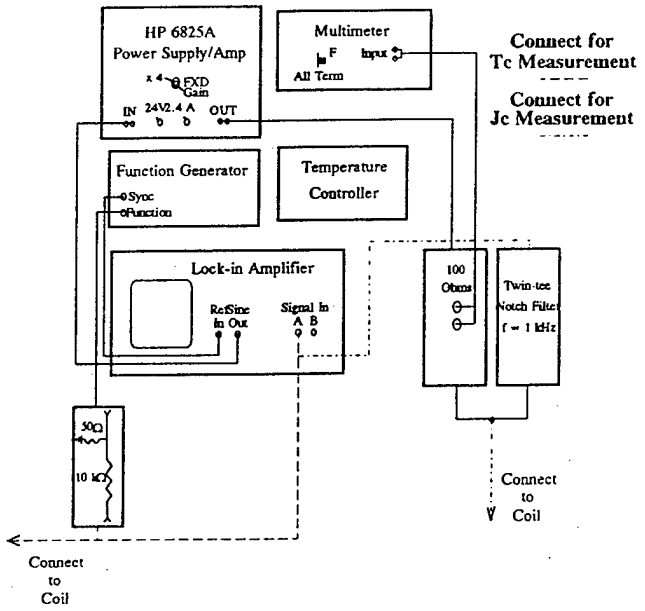

Figure 1. Critical temperature and critical current density measurement system schematic.

III. Results and Discussion

The pre-irradiation critical temperature transitions for the Tl-based films ranged from about 85-113 K and from about 86-90 K for the YBCO films. The pre-irradiation critical current densities at 77 K for all the samples ranged from on the order of 10^4 A/cm^2 up to on the order of 10^6 A/cm^2.

A. Gamma-ray Irradiations

The structures proved to be hard to gamma-rays up to very high doses and exhibited relatively little change in their critical temperature or critical current density characteristics. The measurements were taken 30 minutes after the films were removed from the source. This did not permit short term transient effects, possibly occurring during the irradiations, to be observed.

The critical temperature and critical current density characteristics of a typical sample of YBCO on a $LaAlO_3$ substrate after several gamma-ray irradiations up to a cumulative dose of 1.5 Mrad(Si) are shown in Figures 2 and 3. As shown in these figures, there was very little change in the critical temperature transition region (~89.4 K) or in the critical current density (~1.5 x 10^6 A/cm^2 at 77 K). This was typical for all samples that underwent gamma-ray irradiations and seemed to be independent of the initial quality of the superconductor. The critical temperature and critical current density measurement data for a typical sample of each superconductor/substrate combination that underwent gamma-ray irradiations are listed in Table I.

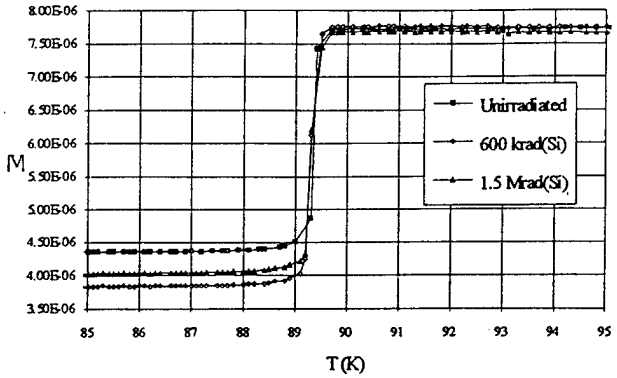

Figure 2. Critical temperature transition of $YBa_2Cu_3O_{7-x}$ on a $LaAlO_3$ substrate after gamma irradiations.

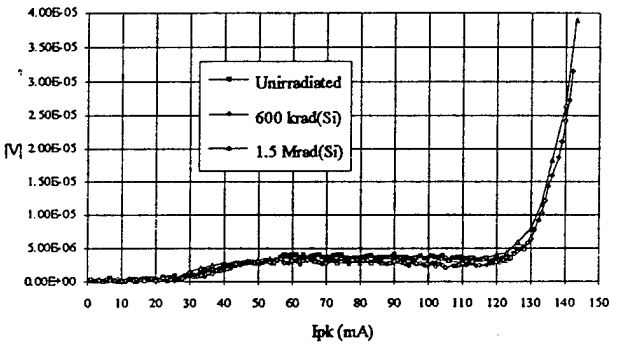

Figure 3. Critical current density measurement of $YBa_2Cu_3O_{7-x}$ on a $LaAlO_3$ substrate after gamma irradiations.

B. Neutron Irradiations

The various sample types were exposed to cumulative neutron fluences up to 10^{14} n/cm^2. An accompanying total gamma dose of 237.9 krad(Si) was also emitted by the Cf-252 source. However, this was neglected knowing that the same types of samples had been exposed to much higher gamma doses with the Cs-137 source. X-ray diffraction analyses failed to show any atomic disorder as a result of the neutron irradiations. In Figures 4 and 5, critical temperature and critical current density measurements of a typical sample of Tl-2212 on an MgO substrate are shown after undergoing neutron exposures. As seen in Figure 5, there was a decrease in critical current density thought to be caused by exposure to moderately humid air for an extended period of time. After exposure to the highest fluences, where longer environmental exposure times (on the order of up to two weeks) were necessary for the samples to radioactively decay, the critical current density degradation, as shown in Figure 6, was

observed. This environmental degradation was confirmed by leaving samples open to the environment for an equal amount of time (two weeks) and then remeasuring the superconductors. Thus, the degradation observed in this work, although similar to that resulting from proton bombardment by Lombardo et al. and Weaver et al. [7,8], is caused by moisture absorption. Critical temperature and critical current density measurement data for samples of each superconductor/substrate combination irradiated with neutrons and exposed to the environment appear in Table II.

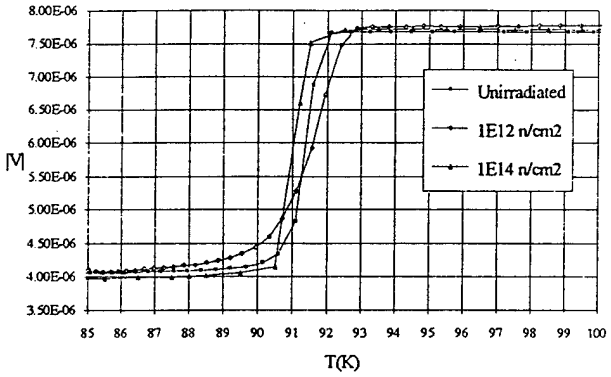

Figure 4. Critical temperature transition of $Tl_2Ba_2CaCu_2O_{8+x}$ on a MgO substrate after various neutron fluences.

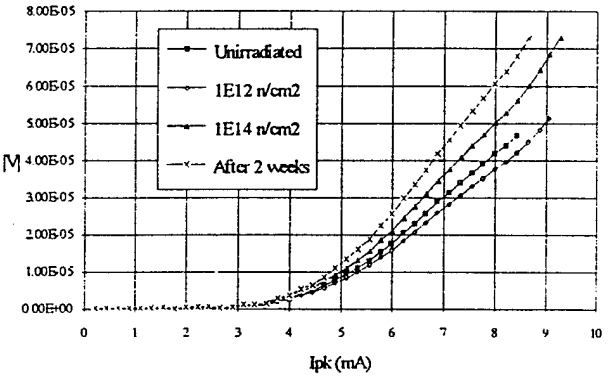

Figure 5. Critical current density measurement of $Tl_2Ba_2CaCu_2O_{8+x}$ on a MgO substrate after various neutron fluences.

Exposure to moisture in the surrounding air had no adverse effects on the critical temperature of YBCO samples, but seemed to have a slight effect on the critical temperature of the Tl-2212 superconductors although it was independent of their initial critical temperature and critical current density values. This is illustrated in Figure 4 where the temperature transition fluctuates slightly and, at 10^{12} n/cm^2, the transition region widens from 2 K to 4.2 K. This may be due to larger grain boundaries in the Tl-2212 film which were deposited by laser-ablation as opposed to sputtering. However, this has yet to be verified.

As shown in Figure 6, further environmental degradation, which can probably be attributed to corrosion taking place at the surfaces of the superconductors from exposure to moderately humid air, occurred [9,10]. Samples of varying thicknesses (other than those listed in Table II) were irradiated to the same neutron fluences. Thickness was determined not to be a factor in our experiments. Unirradiated samples were also exposed to the same environment and showed essentially the same degradation in critical current density with time. No moisture exposure effects were seen up to fluences of 10^{12} n/cm^2, probably because of the short time the samples were exposed to air (approximately 1.4 hours for the exposure time and about 1 day for the decay time). Zhou and McDevitt have shown that Tl-2223 bulk samples tend to degrade more slowly than YBCO bulk samples (by a factor of 3) when exposed to high humidity (85%) with the primary corrosion products being CuO, $BaCO_3$, Tl_2O_3, and $CaCO_3$ [10]. X-ray diffraction analyses were also performed but did not show any detectable levels of atomic disorder as a result of the neutron irradiations. Degradation was not seen during the gamma-ray irradiations because of the much shorter exposure times that involved no radioactivation of the samples. There were no noticeable changes in the temperature transitions of the materials due to irradiations or exposure to air.

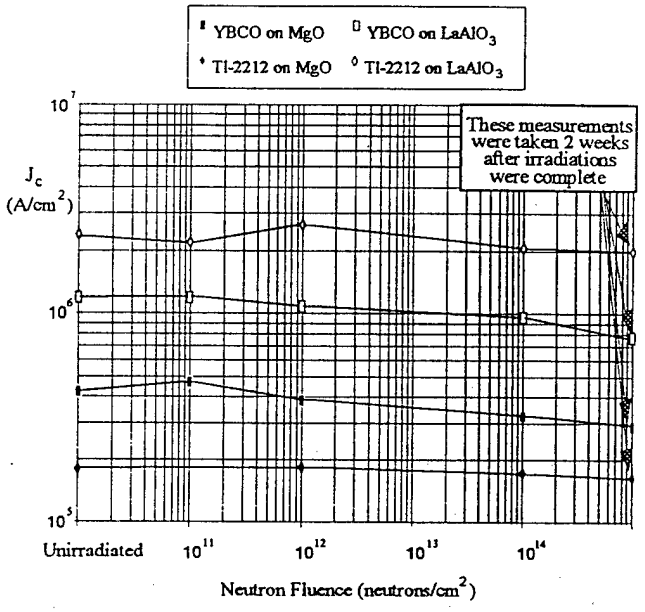

Figure 6. Critical current density variation of various superconductor/substrate combinations for different neutron fluences (also shown is the variation due to air exposure.)

C. *Improvements for Future Studies*

Biasing the superconducting thin films and measuring their characteristics at cryogenic temperatures would have been much more realistic, but this was not possible because of the limitations on the containment necessary for the radiation sources. In particular, the application of a voltage across a dielectric during gamma irradiation is known to enhance degradation of dielectric type materials because of charge creation, separation, and trapping in a dielectric or at a semiconductor/dielectric interface. However, these initial experiments performed at room temperature in air showed that the

Table I. T_c and J_c measurement data for gamma-ray irradiated samples. (J_c values were measured at 77 K.)

HTSC Film	Substrate	Film Thickness (Å)	Unirradiated		600 krad(Si)		1.5 Mrad(Si)	
			T_c(K)	J_c(A/cm^2)	T_c(K)	J_c(A/cm^2)	T_c(K)	J_c(A/cm^2)
YBCO	MgO	~2000	82.6	7.2×10^4	82.6	8.4×10^4	82.6	6.6×10^4
YBCO	$LaAlO_3$	~10,000	89.4	1.54×10^6	89.4	1.51×10^6	89.4	1.49×10^6
Tl-2223	MgO	~3000	112	6.0×10^4	112.3	9.6×10^4	111.6	7.6×10^4
Tl-2212	$LaAlO_3$	~5000	86.2	1.92×10^6	86.4	1.87×10^6	86.5	1.87×10^6

Table II. T_c and J_c measurement data for neutron irradiated samples. (J_c values were measured at 77 K.)

HTSC Film	Substrate	Film Thickness (Å)	Unirradiated		10^{12} n/cm^2		10^{14} n/cm^2		J_c (2 weeks after irradiations) (A/cm^2)
			T_c(K)	J_c(A/cm^2)	T_c(K)	J_c(A/cm^2)	T_c(K)	J_c(A/cm^2)	
YBCO	MgO	~2000	84.2	4.2×10^5	84.5	3.84×10^5	84.4	3.24×10^5	2.88×10^5
YBCO	$LaAlO_3$	~10,000	89.5	1.19×10^6	89.6	1.08×10^6	89.5	9.6×10^5	7.68×10^5
Tl-2212	MgO	~3000	91.3	1.8×10^5	91.6	1.84×10^5	91.0	1.72×10^5	1.64×10^5
Tl-2212	$LaAlO_3$	~5000	102.6	2.38×10^6	102.9	2.64×10^6	102.9	2.06×10^6	1.99×10^6

superconducting thin film structures are hard to the levels of radiation described. Such information is a necessary initial step in understanding how superconducting multichip modules will perform in a radiation environment.

IV. Conclusions

Gamma-rays and neutrons had little to no effect on the critical temperature and critical current density of thin films of YBCO, Tl-2212, and Tl-2223. Since these properties of superconductors are highly sensitive to atomic displacement effects in the material, it can be concluded that very little damage occurred in the unbiased superconductors at room temperature as a result of the irradiations performed. Although the outcome may have been different if the films were biased and were irradiated and measured at 77 K, the results presented here are encouraging.

It was also determined that the films were more susceptible to degradation by the environment than by radiation. The results suggest that the surrounding air and humidity caused a decrease in the critical current density of the materials due to surface corrosion [9,10].

As mentioned previously, we are currently working on the development of a multichip module utilizing superconducting interconnects. If our efforts are successful, it will be of great interest to perform radiation experiments on such a device to gain some insight into its hardness to space radiation effects. The experiments performed here have provided a good foundation for making a more detailed study on such a superconducting device.

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A Comparison of High-Temperature Superconductors in Multi-Chip Module Applications

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Abstract

In the application of high-temperature superconductors (HTSCs) in multi-chip module (MCM) technology, it is first necessary to investigate the advantages and disadvantages of the various HTSC compounds. The standard criteria for comparing the suitability of HTSCs in electronics applications has been critical temperature (T_c) and critical current density (J_c). It is also necessary to consider the physical properties of HTSCs in relation to the various processing techniques required in fabrication of MCMs. These techniques can be grouped into four main areas: deposition, patterning, packaging, and characterization. The four main HTSC materials, Y-Ba-Cu-O, Bi-Sr-Ca-Cu-O, Tl,Ba-Ca-Cu-O and Hg-Ba-Ca-Cu-O, will be compared to determine which is most suitable for MCM application.

Introduction

In the decades since the popular advent of the transistor in the 1960s, there has been continual and steady improvement in both the performance and cost of electronics equipment through miniaturization. This effort has given us the multi-chip module (MCM) as the latest and most promising technique to be introduced. MCM technology improves the speed at which devices can operate and decreases the power lost by eliminating as much length as possible from the interconnection between the individual devices. With this new technology some new barriers to increased speed and performance have arisen. By concentrating all of the devices in one area, the problems due to Joulean heating (I^2R losses) and electromigration are increased. Also, the lack of recent improvements may indicate that the upper limit of the speeds that can be expected from current semiconductor devices using conventional interconnects have been reached.

All of these problems can be addressed by combining high-temperature superconductors (HTSCs) with MCMs. Some of the interconnecting lines may typically carry 50 - 100 mA of current. Therefore, they account for a major portion of the heat generated (Burns et al., 1993). Replacing the lines with zero resistance HTSCs eliminates these I^2R losses. This means less heat and less power consumed. The refrigeration required for HTSC operation further limits the overall heat production to less than that produced by the individual devices. All of this allows for an even greater decrease in the interconnection lengths which, in turn, maximizes the operating speed of the MCM.

HTSC devices have been shown to be more than 2.5 times faster than their semiconductor counterparts, use three orders of magnitude less power, and do not suffer from electromigration problems (Van Duzer and Tuner, 1981). Their use in MCMs should produce the next quantum jump in performance. A cross-sectional schematic of an MCM is shown in Figure 1.

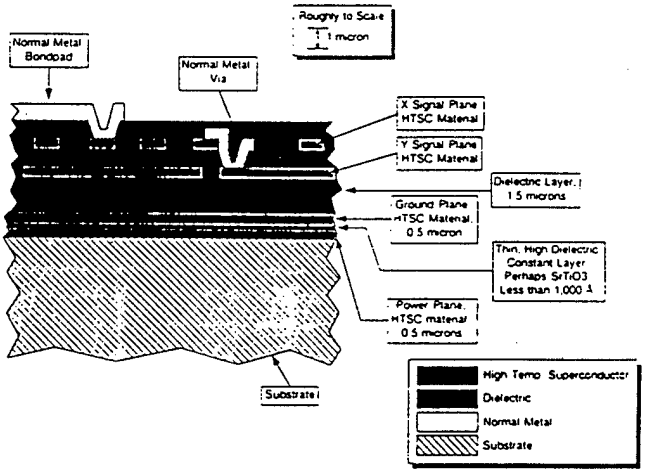

Fig. 1. Cross-sectional Schematic of a Superconducting Multi-Chip Module.

But, which HTSC offers the best overall prospects for MCM applications? This is the first question to be answered in the search for a viable superconducting MCM. When comparing HTSCs, the standard for suitability in electronics applications has been the materials critical temperature, (T_c), and critical current density, (J_c). It is

also necessary to consider the additional requirements and effects due to the different fabrication steps such as erial deposition, patterning, packaging and characterization. This paper is the result of our research in each of these areas.

Using the initial criterion of T_c, a great number of HTSCs can be eliminated. The cost of cooling below liquid nitrogen temperature (77K) tends to preclude using HTSCs with T_c's any lower. The currently viable HTSC materials with T_c's above liquid nitrogen temperature can be separated in to four groups: yttrium-based, bismuth-based, thallium-based, and mercury-based. These four groups will be dealt with in this paper.

Yttrium

There are at least three variations to the yttrium-based HTSCs with the only significant differences being the T_cs (40K, 80K, 90K) and the ease of production. Fortunately, the highest T_c (90K) belongs to the phase of yttrium material that is the easiest to produce. $YBa_2Cu_2O_x$, known commonly as either YBCO or 123, was the first material discovered to superconduct above liquid nitrogen temperature (Wu et al., 1989). This fact and the relatively low toxicity of the component materials seem to be the only really good characteristics that YBCO possesses.

An ongoing study by our group at the University of kansas indicates that to achieve an effective current den-, a given HTSC must be held to 10 - 20% below its T_c (Ulrich, 1994). While this is better than the 30% or $T_c/2$ values commonly accepted in the scientific community (Doss, 1989), it still puts YBCO at the very borderline for use with liquid nitrogen.

Most of the drawbacks encountered in the production of YBCO thin films can be tied to one problem. Due to critical mismatches in lattice parameters, it is difficult to get good epitaxial growth for YBCO on the viable low dielectric substrates in use today (Werder, 1991). This means that, no matter how good a deposition technique, YBCO films will tend to be comparatively rough in texture and have a limited J_c due to internal flaws in the achievable crystalline structure.

The deposition of YBCO on a substrate has typically been accomplished using off-axis sputter deposition. While this method can produce usable thin films, it is often necessary to anneal these films in an oxygen ambient at approximately 450°C after deposition in order to correct for oxygen depletion and to achieve an acceptable T_c. Fortunately, an on-axis method has been demonstrated that produces thin films with T_cs of 88K and J_cs of greater than 10^6 A/cm^2 with no post annealing required (Blue and Boolchand, 1991). It should be noted however, that the current density for this material is only 10^4 A/cm^2 at 77K as for most YBCO films (Jin et al., 1988).

Another successful method for the deposition of YBCO has been demonstrated using metalorganic chemical vapor deposition (MOCVD) combined with rapid isothermal processing (RIP) (Singh et al., 1991). With T_cs of 89K and J_cs of 1.5 x 10^6 A/cm^6 at 77K, this is by far the best method for producing YBCO films seen to date.

Pulsed laser deposition has also been used successfully to cover small areas, but this technique has proven to be a very costly and a difficult process to control (Burns et al., 1993). Laser deposition does seem to be an excellent choice for spot deposition of YBCO in applications such as individual connections between layers commonly called vias.

In the areas of patterning, packaging and characterization, there is another major drawback. YBCO has a very high affinity for water. When exposed to moisture, the properties of YBCO tend to degrade. This process is accelerated by flaws in the crystalline structure so common to current processing techniques. Another aspect of this fault is that YBCO tends to form an oxide skin layer. This means an added difficulty for any patterning process. Also, this creates a problem in making direct contact to YBCO films as is necessary for multilayer applications, metalization for packaging purposes, or just testing the material. With some small difficulty, this can be dealt with using a procedure consisting of a solution of bromine in methanol that will remove the skin layer (Vasquez et al., 1988). A non-superconducting surface layer can also be removed by brief exposure to a low-energy cleaning ion bombardment.

Yttrium-based HTSCs have been successfully etched using weak acidic solutions such as phosphoric, nitric and hydrochloric acids. However, YBCO's reactivity with the various substrates, while not notably greater than for other HTSCs, when combined with the noted skin effect creates a scum layer between the substrate and the YBCO thin film that seems impervious to these enchants.

Yttrium-based HTSCs can also be dry etched using either a reactive process with a halogen such as chlorine, or by argon ion milling. Both of these methods suffer from the same structural distortions found in deposition techniques. For the reactive process, it is necessary to either post-etch anneal or use a mask that can keep oxygen from escaping during the etching process. In argon ion milling, the problem can be solved by cooling the sample during the etching process, preferably with liquid nitrogen. But, since photoresist are often used for masking in both dry etching processes, the problem with moisture is still present.

Bismuth

There are several different bismuth based HTSCs, with

the highest T_c being ~114K for $Bi_2Sr_2Ca_2Cu_3O_x$, but it is very difficult to produce the higher T_c phase of this compound (Bi 2223). This is due to the intergrowth of the Bi 2212 phase which has a T_c of 85K. Many attempts to enhance growth of the 2223 phase have been made with varied results (Endo et al., 1988; 1989; Tarascon et al., 1988; Huang et al., 1990). One procedure produces good thin films, but requires a heating period of one week (Sleight, 1988). The most promising method seems to be the addition of lead in the form $Bi_{2-y}Pb_ySr_2Ca_2Cu_3O_x$ to stabilize the Tc. This method has produced T_cs in the usable range of 104 - 112K (Xin and Sheng, 1991). This is the most commonly encountered form of the bismuth compound and can be deposited using the same methods as described for YBCO. Most of the information gathered about the bismuth-based system has been for this lead mixed form. As other easily produced phases of the bismuth compound have lower T_cs than YBCO, they are of little interest to the MCM field.

The addition of lead to bismuth HTSCs defeats one of the bismuth compound's major benefits. That is, the relatively low toxicity of the elements used. While the lead can be incorporated easily, it will still require special handling like the thallium and mercury compounds.

Most reports of J_cs are somewhere above 10^4 A/cm^2 at 77K which is similar to YBCO (Doss, 1989). This is probably due, in part, to the difficulty in producing a pure phase of this material. The lattice parameters of the bismuth compounds, though not exact, are better matched to the low dielectric substrates than YBCO's. This would indicate better epitaxial growth and better J_cs. Comparison of the thermal power properties also indicates this conclusion (Xin et al., 1992). Indeed, a 110K sample with a J_c of 3.4 x 10^6 Z/cm^2 at 77K has been reported (Grenwald, 1991), but it should be noted that this sample did not contain lead and is not easily reproduced.

Bismuth-based HTSCs can be etched with the same methods as YBCO and slow none of the problems due to YBCO's affinity for moisture. Most forms of this compound appear to be fairly stable and much less brittle than YBCO. It should be noted that bismuth compounds require the same precautions for dry etching methods as YBCO, and although the etching damage is generally of a lesser extent, bismuth compounds can easily be destroyed during any annealing process.

Bismuth compounds have shown a tendency to flake in layers similar to mica (Doss, 1989). This could cause some slight problems in packaging, but should not prove to be a major concern.

The only problems with the characterization of bismuth based HTSCs are directly related to the ability to produce a pure phase material.

Thallium

Like bismuth, thallium-based HTSCs exist in many (ferent phases. Unlike bismuth, however, the highest (125K) phase is relatively easy to produ $Tl_2Ba_2Ca_2Cu_3O_x$, commonly referred to as Tl2223, l one major drawback. Thallium is a very toxic substan that can be absorbed through the skin. It can be absorb over a period of time and is not normally purged from t body. Therefore, proper precautions must be taken wh dealing with this material. Special precautions should taken when working with lead or mercury. However, t precautions required for working with these materials a only slightly more than those normally observed in a co scientious production facility (Chelton et al., 1991). these facilities are already dealing with arsenide, cyanid and many other toxic compounds, the addition of thalliu should present no insurmountable problems.

Excellent quality thin films of the 2223 phase have be deposited by several methods such as spin coating, spr pyrolysis, sputtering, thermal evaporation, electron bear laser ablation, and MOCVD (Shih and Qiu, 1988; Ichika et al., 1988; Ginely et al., 1989; Hammond et al., 199 Collins et al., 1991; Liu et al., 1991; Malandrino et a 1991), but the method of choice seems to be the po deposition annealing technique. First, a precursor layer BaCaCuO of the desired stoichiometry is sputter depos ed onto a substrate. Then the film is annealed in thalliu vapor which drives the thallium into the matrix formir the actual HTSC. While a one step sputter deposition possible, the two step method consistently provides bett results with average T_cs of 125K and J_cs typically above 1(A/cm^2 at 77K (Grenwald, 1991). This includes the be quality samples to date with a J_c of over 10^7 A/cm^2 at 77 (Chu et al., 1991). The two step method may also have hidden benefit in that it isolates thallium contamination t the furnace used for the drive-in procedure.

The lattice parameters for the 2223 phase are muc closer to those of the low dielectric substrates with as litt as 0.75% mismatch for CeO_2 (Holstien et al., 1992). Thi means better epitaxial growth and smoother films tha possible with either YBCO or bismuth (Lee et al., 1992).

Thallium-based HTSCs can be etched using the sam methods as yttrium-based and bismuth-based compounds but because of the greater stability, require less attentio to reactivity and oxygen loss. The preliminary results fron a wet etch process our group is currently investigatin indicates that the extra strength and consistency of 222 films makes the etching process much easier to control.

Other than the special precautions for dealing wit thallium 2223 makes no special demands on packaging o characterization. Indeed, the additional strength can onl serve to make these processes easier. A comparison of T curves for Yttrium, Bismuth and Thallium superconduc

tors is shown in Fig. 2.

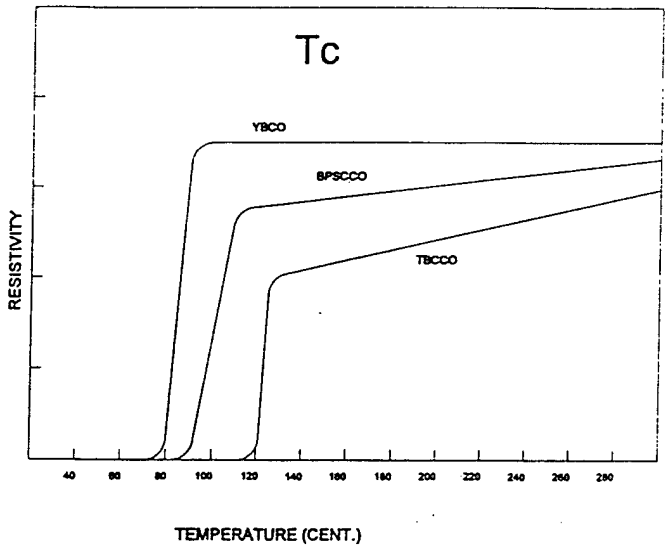

Fig. 2. Comparison of Typical T_c Curves.

Mercury

The recent discovery of mercury based HTSCs with possible T_cs above the 145K boiling point of Freon™ is ...ly exciting. But, as of yet, little is known of the characteristics of the mercury-based compounds. The $HgBa_2Ca_2Cu_3O_x$ phase (Hg 1223) with the highest T_c of 135K at ambient pressure has been shown to increase to a T_c of over 150K under hydrostatic pressure (Chu et al., 1993). However, 1223 is not produced without some amount of effort. 1223 thin films have currently been produced only by post deposition annealing under special pressure controlled conditions. With the additional cost due to current government efforts to ban the use of Freon™, the added effort necessary to produce the material and then maintain the hydrostatic pressure, means that practical Freon™-cooled HTSCs are still far in the future. Indeed, the added effort required just to achieve an additional 10K increase in T_c from thallium's 125K to 135K seems to serve no purpose, but improvements could be just over the horizon.

The reported lattice parameters combined with the initial troubles in separating out the different phases, tend to indicate that 1223 will have a J_c somewhat less than the thallium-based HTSCs (Huang et al., 1993), but this remains to be confirmed. The bottom line with mercury-based HTSCs is that we just don't know yet. A comparison of the J_c's of the four materials is shown in table 1.

Table 1. Critical Current Density (J_c) in A/cm².

	YBCO	BSCCO	TBCCO	HBCCO
TYPICAL	10^4	10^4	10^6	?
MAXIMUM	1.5×10^6	3.4×10^6	2.8×10^7	?

Summary and Conclusion

Yttrium base HTSCs, while having several drawbacks, have only one advantage. The comparatively low toxicity of the component materials. While, bismuth-based HTSCs have much more to offer than the yttrium based compounds, the current production of viable bismuth thin films requires the additional of lead. This tends to nullify any benefits relative to thallium-based HTSCs. Most processes used in MCM production have been demonstrated for thallium HTSVs with significantly better results than any other material. Mercury-based materials have shown some prospects and raised some new questions, but until they can be produced with more ease and characterized more definitively, they offer no apparent advantages. However, they definitely warrant more research.

While the evidence does not totally rule out any of the candidate HTSCs, the majority of the information indicates that thallium-based HTSCs should be the HTSC of choice in MCM applications.

Acknowledgements

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The effects of rapid thermal annealing on the properties of sputtered YBCO superconducting films

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Abstract. The effects of rapid thermal annealing on the material and electrical properties of sputter deposited yttrium barium copper oxide ($YBa_2Cu_3O_{7-x}$) superconducting films were investigated. Rapid thermal annealing increased the critical current density but decreased the critical transition temperature of the films. The maximum increase in critical current density, an order of magnitude, occurred at 800 °C, while no increase was observed at 700 °C, below the growth temperature of 735 °C, or at 900 °C. The increase in critical current density is due to a reduction in the density of misaligned grains as evidenced by a decreasing *c*-axis parameter and a decrease in the full width at half maximum (FWHM) of the (005) peak. The critical temperature decreased for all annealing times and temperatures above the growth temperature due, presumably, to oxygen effusion from the films.

1. Introduction

Thin superconducting yttrium barium copper oxide (YBCO) films have been grown by various techniques including ion-beam sputtering [1], magnetron sputtering [2], electron-beam evaporation [3], molecular-beam epitaxy [4], metalorganic chemical vapour deposition [5], and laser ablation [6]. Most of these techniques require either post-deposition oxygen annealing or growth at an elevated substrate temperature to convert the YBCO films from the tetragonal phase to the orthorhombic phase. In order to optimize post-deposition annealing conditions, it is necessary to understand the thermodynamics of the structural and chemical changes that occur during annealing. Davidson *et al* [7] investigated the resistance of e-beam-evaporated as-deposited $YBa_2Cu_3O_{7-x}$ films with different heating rates and O_2 partial pressures. They reported that fast annealing is preferable over slow annealing in converting the as-deposited $YBa_2Cu_3O_{7-x}$ into an orthorhombic-phase superconducting film.

In order for superconducting thin films to be used in electronics, they must undergo numerous processing steps such as patterning, etching, and subsequent depositions and passivation. It is generally known that processing steps, performed subsequently to the deposition of superconducting thin films, have a pronounced effect on their material and electrical properties. Sheats *et al* [8] reported severe degradation in the critical current density (J_c) of multitarget-sputtered YBCO films to less than 4% of the initial value after a small amount of ion milling (approximately 375 Å). They also found that a conventional photoresist bake at 105 °C resulted in as much as a 94% decrease in the J_c. Ichikawa *et al* [9] found that the J_c of their sputtered YBCO films degraded after overcoating with aluminum oxide, Al_2O_3, by sputtering. They attributed this degradation to the interdiffusion between the YBCO and dielectric, which modified the crystal structure of the YBCO films. In general, the J_c of YBCO films has been observed to degrade severely with post-deposition processing [10], although some modest increases in J_c after processing have been reported [11].

Rapid thermal annealing (RTA) has been shown to be a viable processing technology by which thermal annealing is performed for a short duration, usually for a few minutes or less. The main advantage of RTA is a reduced thermal processing budget. The reduced thermal budget mitigates interdiffusion problems associated with the YBCO/dielectric layers. This is especially beneficial in the fabrication of superconducting multichip modules (MCMs) where at least two layers of YBCO interconnects, sandwiched between a thick dielectric, are required.

RTA was investigated in this work as a potential process for improving the electrical characteristics of YBCO films. In this paper, the effects of RTA on the material and electrical properties of sputtered YBCO thin films are reported. In addition, the effects of post-RTA annealing at a low temperature in an O_2 ambient on the transition temperature (T_c) of these films are also discussed.

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2. Experimental details

YBCO films were deposited by off-axis DC magnetron sputtering from a two-inch-diameter stoichiometric $Y_1Ba_2Cu_3O_{7-x}$ target. The substrates used were polished 1 cm^2 yttria-stabilized zirconia (YSZ) of (100) orientation. The deposition parameters were as follows: base pressure, 10^{-6} Torr, deposition pressure, 200 mT with 80% Ar and 20% O_2, substrate temperature, 735 °C, and sputter power, 100 W. A deposition rate of about 1000 Å h^{-1} was achieved using these parameters, and nominal film thicknesses were 4000 Å. After deposition, the films were cooled in 100% O_2 at about 600 Torr and held at 400 °C for 30 min before being ramped down to room temperature. The total cooling time was about 2 h.

Two different groups of films, referred to hereafter as group A and group B, were annealed using a computer-controlled Heatpulse 210-T rapid thermal processor. Each film was placed on a two-inch silicon wafer for support inside a double-walled quartz furnace. The annealing temperature was measured using a type-K thermocouple pressed against the surface of the film. Films were annealed at temperatures ranging from 700 °C to 900 °C in 50 °C increments; sample group A was annealed for 10 s, and sample group B for 30 s. A fresh film was used for each annealing increment. Annealing and cooling were performed in the presence of 50 sccm of oxygen (limited by the volume of the furnace), and were allowed to cool to 200 °C before being removed from the furnace. Typical cooling times required were about 5 min for the 10 s annealed films and about 7 min for the 30 s annealed films. Some samples were O_2 annealed at a low temperature after RTA. The annealing temperature was ramped up to 450 °C in 30 min and held at this temperature for 2 h under 700 Torr of O_2. The samples were then cooled to room temperature in about 1 h.

A contactless method was used to measure the J_c and T_c of the films. In this technique, the sample is placed between two coils and then cooled to 77 K. A current is passed through one of the coils, which induces current flow in the film. The other coil detects the signal produced when J_c is exceeded [12]. This technique has the important benefit of not requiring patterning of the films in order to perform the measurement. Furthermore, it is only sensitive to intergranular critical current. The transition temperature of the sample is measured by the reactive component of the coil voltage at the fundamental drive frequency, as the inductance drops substantially at the transition temperature due to the induced shielding current in the film. The YBCO films were also analysed using a Philips PW-1830 x-ray diffractometer (XRD) equipped with a Eulerian cradle. The *c*-axis parameters were measured using the *d*-spacing of the (0011) peaks located near $2\theta = 92.5°$ to minimize systematic errors of the diffractometer. Rocking curves about the (005) peak were also observed. This peak was selected because of its relatively high intensity. The starting and finishing θ angles were 18° and 21°, respectively, with a step size of 0.01° and a dwell time of 1.5 s/step. The fixed 2θ position of the detector was determined by noting the maximum intensity. Furthermore, the collimating slit in front of the detector was removed to maximize detected diffraction. All XRD measurements were performed at 27 °C.

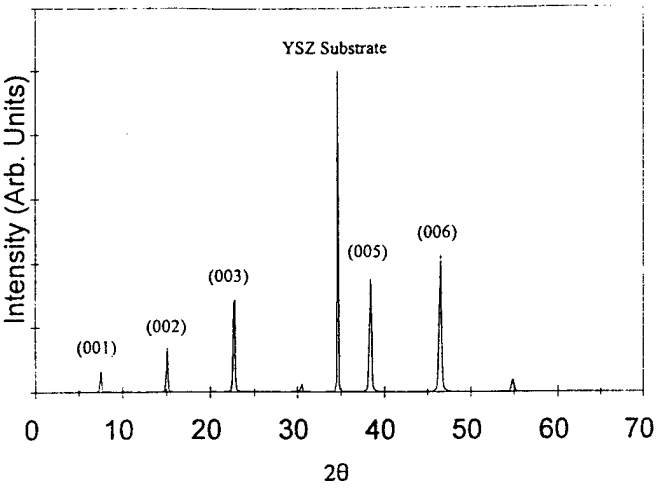

Figure 1. The XRD pattern of a typical as-deposited YBCO film.

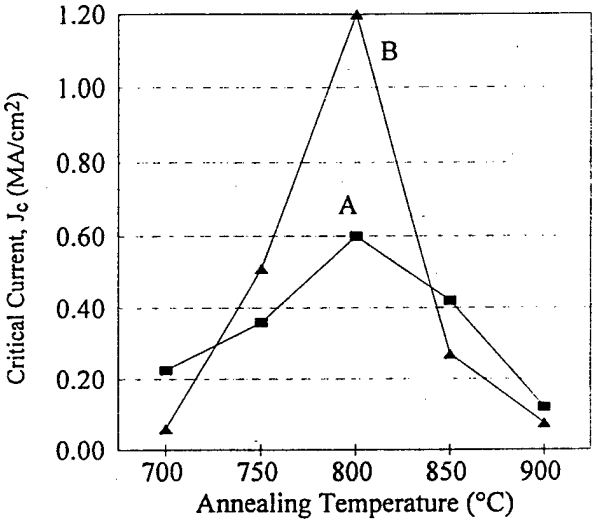

Figure 2. Critical current density versus annealing temperature plots for groups A and B of the YBCO samples.

3. Results and discussion

All of the as-deposited YBCO films yielded very uniform T_c and J_c data, due to the excellent repeatability of the deposition parameters. The mean value of T_c and J_c for both groups of films was 85 K and 1.4×10^5 A cm^{-2}, respectively. Figure 1 shows the XRD pattern of a typical as-sputtered film. As can be seen, the strongest peak intensity occurs for the (006) peak. The (020) peak is much smaller in intensity than the peaks corresponding to *c*-oriented grains. Thus, the predominant growth is *c*-axis-oriented grains.

Figure 2 shows J_c-versus-annealing-temperature curves for both groups of samples. No change in J_c is noted for films annealed at 700 °C, which is below the

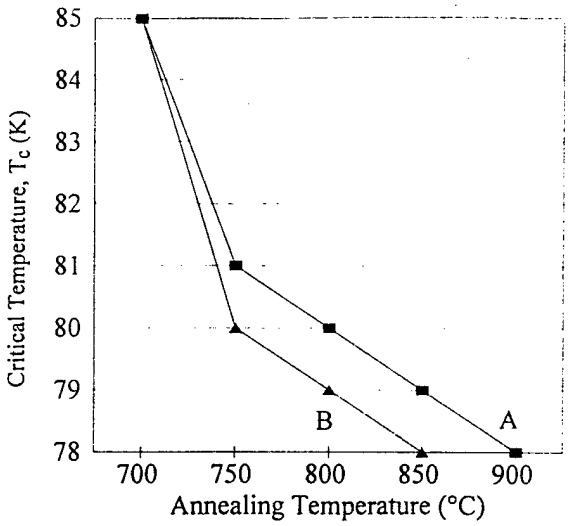

Figure 3. Critical transition temperature versus annealing temperature plots for groups A and B of the YBCO samples.

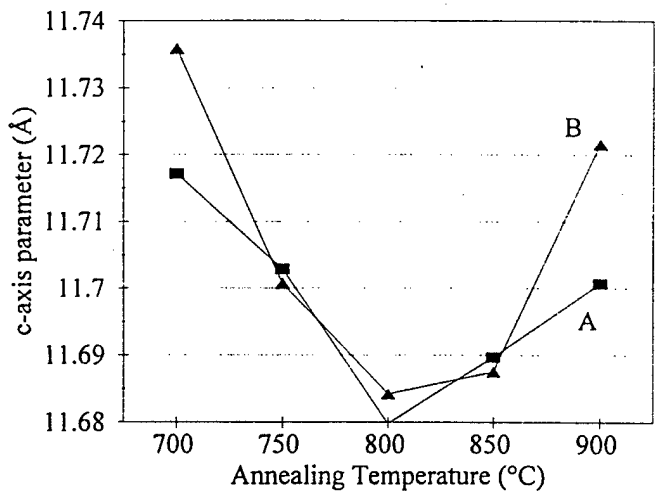

Figure 4. The *c*-axis parameter of the YBCO films as a function of annealing temperature.

deposition temperature of 735 °C. Above the deposition temperature, the J_c of the annealed films increases to a maximum at 800 °C for both groups. The J_c of the sample subjected to a 30 s annealing at 800 °C increases from 1×10^5 A cm^{-2} to about 1.2×10^6 A cm^{-2}. The amount of increase in J_c with annealing then decreases for annealing temperatures above 800 °C. At 900 °C, no increase and, in fact, a slight degradation in J_c is observed. Also, annealing for longer durations (60 s and 90 s) resulted in smaller increases in J_c. While the J_c of these films increases with annealing, their T_c decreases for all annealing times and temperatures. Figure 3 shows the reduction in T_c for annealed films. No change in T_c is noted for films annealed at 700 °C. However, a sharp decrease in T_c (from 85 K to 81 K) is noted for films annealed at 750 °C for 30 s. Furthermore, films annealed for 30 s show a larger decrease in T_c than those annealed for 10 s at all anneal temperatures. The T_c of the 800 °C, 30 s annealed sample recovered to its original value after O_2 annealing at 450 °C for 2 h.

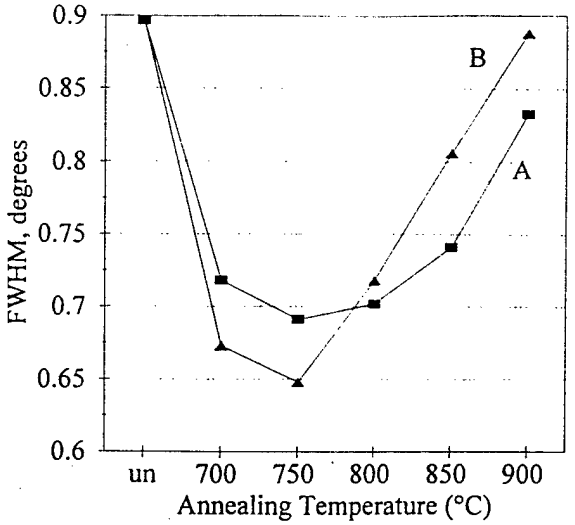

Figure 5. The FWHM versus annealing temperature for groups A and B of the YBCO samples.

Figure 4 shows the *c*-axis parameter of the films as a function of annealing temperature. The *c*-axis lattice parameter decreases from 11.74 Å to 11.69 Å upon annealing at 800 °C for 10 s. Even though only a small change in the *c*-axis parameter is noted, the data indicate that the *c*-axis parameter generally decreases with annealing with a minimum occurring at 800 °C for both anneal temperatures. For temperatures higher than about 800 °C, the decrease in the *c*-axis parameter with annealing is smaller. For example, the *c*-axis parameter decreases from 11.72 Å to about 11.7 Å for the film annealed at 900 °C for 30 s. Reduction in the *c*-axis parameter is indicative of a reduction in grain misalignment. According to Jorgensen *et al* [13], a reduction in the *c*-axis parameter is accompanied by an increase in T_c, and thus, is also a measured of increased oxidation. However, all of our data reveal that a decrease in *c*-axis parameter is accompanied by a decrease in T_c. This may be attributed to lattice strain, since it is well known that, in general, RTA imparts strain to films.

Rocking curves of the (005) peak were obtained using the XRD. The full width at half maximum (FWHM) for each film was measured and is plotted in figure 5. YBCO films of similar thickness (i.e., 4000 Å) were used to facilitate comparison. The FWHM is a direct measure of the number of misaligned grains present in the film and is, therefore, useful for quantifying the amount of misalignment. It is interesting to note that, while no change in T_c or J_c is noted for films annealed at 700 °C (below the deposition temperature of 735 °C), the FWHM decreases from 0.9° for the unannealed film to 0.73° for 10 s annealed films or 0.67° for 30 s annealed films. This indicates that minute restructuring of the films occurs at this annealing temperature resulting in a reduction in the density of misaligned grains. As the figure indicates, the amount of misalignment decreases for all annealing temperatures with a minimum occuring for 750 °C. However, the decrease in misalignment as a function of annealing temperature is smaller for 800 °C and higher temperatures.

Improvement in J_c after RTA can be attributed to a decrease in the density of misaligned grains or a

reduction in the density of weak links [14]. RTA at a temperature higher than the deposition temperature increases the atomic mobility in the as-deposited YBCO film. Eom *et al* [15] reported that, given sufficient mobility at a high temperature, *c*-axis grain growth is favoured over *a*-axis grain growth. The high mobility of the atoms favours *c*-axis growth and deters nucleation of *a*-axis grains. Thus, the decrease in *c*-axis parameter and FWHM of the (005) peak indicate an increase in the density of *c*-axis grains. Scanning-electron-microscope (SEM) photographs of all the annealed films indicate larger grain sizes for the films annealed at higher temperatures, which further suggests a reduction in misaligned grains [16]. The smaller increase in J_c for annealing at temperatures above 800 °C is possibly due to partial eutectic melting at these temperatures [3].

The decrease in T_c with RTA is probably attributable to the loss of O during annealing. Since RTA was performed at atmospheric pressure, O can easily effuse from the film [17]. O effusion is more pronounced for films annealed for a longer duration as indicated by the lower T_c of these films. Annealing in an O_2 ambient at 450 °C did have the effect of restoring the T_c of these RTA-annealed films to nearly the original values, supporting the assumption that O effusion occurs during RTA. Unfortunately, the J_c values were also reduced, but they remained higher than their original values.

4. Summary and conclusions

RTA was performed on superconducting YBCO films at temperatures ranging from 700 °C to 900 °C, and for 10 and 30 s durations. A general increase in J_c occurred, with the greatest increase, a factor of 10, occurring at an anneal temperature of 800 °C for 30 s. For all times and tempertures, T_c decreased, which is attributable to O effusion from the films. Measurements of the FWHM of the (005) peak and the *c*-axis lattice parameter indicate that the increase in J_c is due to a decrease in the number of misaligned grains present in the film. The reduction in T_c with RTA was reversed by conventional low-temperature annealing in O_2. However, this also caused J_c to decrease although the final values were greater than the as-deposited values.

Acknowledgments

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THE EFFECTS OF LOW-ENERGY BLANKET ION MILLING ON THE PROPERTIES OF SUPERCONDUCTING YBCO FILMS

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ABSTRACT

The effects of low-energy blanket ion milling on the electrical and structural properties of superconducting yttrium-barium-copper-oxide ($YBa_2Cu_3O_{7-x}$, or YBCO) were investigated. This process has proven not to have a detrimental effect on the electrical or structural properties of high-quality YBCO films. In fact, it has been found that, in many cases, the critical current density (J_c) improves as a result of a brief exposure to a low-energy ion beam. Also, milling of high-quality films results in a reduction in RMS surface roughness. Lower-quality films are typically degraded by the same process.

INTRODUCTION

The High-Density Electronics Center (HiDEC) at the University of Arkansas is conducting research directed at the fabrication of superconducting multi-chip modules (MCMs). These modules will consist of semiconducting ICs on a superconducting interconnect structure. The superconductor material of choice is YBCO. Due to the reactivity of YBCO with air and water, its surface develops a non-superconducting layer through processing and handling. It is desired that this layer be removed prior to metallization (preferably in-situ) to produce a low-resistance contact. Ion milling is under consideration to serve this purpose. Consequently, the effects of ion bombardment on the electrical and structural properties of YBCO must be investigated to determine the effectiveness of this process.

The proposed superconducting MCM interconnect structure consists of two superconducting planes separated by dielectric layers which are deposited on a substrate. This two-layer structure is based on the interconnected mesh power system (IMPS) MCM topology [1], in which the power, ground, and signal components are combined into two planes. Due to the high dependence on the crystallographic properties when interfacing ceramic materials, minimization of layers is critical in this structure.

The four-sided problem of lattice matching, coefficient of thermal expansion

See presentation

(CTE), interdiffusion, and dielectric constant prevent the use of a single material for the dielectric layer in this structure. The currently proposed dielectric layer for the HiDEC superconducting MCM consists of silicon oxide (Si_xO_y) buffered by layers of cerium dioxide (CeO_2) grown either by an ion beam assisted sputtering or laser ablation technique. Si_xO_y has been chosen due to its low dielectric constant, and its extensive application in electronics. The Si_xO_y will be tailored by sputter deposition for the best trade-off between its dielectric constant and CTE. CeO_2 has been chosen to buffer between Si_xO_y and YBCO because of its lattice parameter and CTE match with YBCO.

The superconductor planes are to be connected by metal vias. Previous publications have illustrated the severe degradation of the critical current density (J_c) of a superconducting YBCO via [2]. This reduction in J_c is due to the anisotropic nature of current flow in YBCO [3]. In order to keep the YBCO layers planar, the Si_xO_y will be planarized prior to the second YBCO deposition, and the YBCO layers will be connected by reach-through vias. The ideal metal for low-resistance contact to YBCO is gold (Au). Other options are silver (Ag), platinum (Pt), or a multi-layer metal. A cross-sectional representation of the superconducting MCM interconnect structure is shown in Figure 1.

An item of extreme importance, not considered in the previous section, is that of the reactivity of YBCO with its surroundings. YBCO has been shown to be reactive with many of its environmental components, especially air and water [4-6]. This results in the formation of a non-superconducting surface layer on YBCO films upon exposure to air and conventional wet processing steps, such as photolithography. This reacted layer results in higher-resistance contacts and defeats the purpose of lattice matching at the interface of a dielectric and a reacted YBCO surface. Avoidance of these reactions by shielding YBCO from a reactive atmosphere would be very time consuming as well as expensive. Figure 2 shows the interconnect structure of Figure 1 taking into account a non-superconducting surface on the YBCO planes of the superconducting MCM interconnect structure.

EXPERIMENTAL PROCEDURES

Removal of the non-superconducting surface of YBCO is the most feasible solution to the reactivity problem. It is desirable for this removal process to be performed in the same chamber as the subsequent deposition step, so that the superconducting surface of the YBCO is not exposed to air. In the fabrication of the HiDEC module, where the CeO_2 layers are deposited by ion-beam assisted sputtering in the same chamber in which metallization is performed, the ion source may be used to etch the YBCO films until the superconducting bulk is exposed. This arrangement then allows for the deposition of the dielectric layer or metal following the in-situ milling process.

The use of inert ions to bombard a surface in order to remove material is called ion milling. Ion milling has been applied extensively to the patterning of YBCO films [7,8]. However, it has also been reported that it degrades the electrical properties of

YBCO [9]. Since the surface preparatory process exposes the entire surface of the film (this is where the term "blanket" comes from), a major concern is damage to the remaining film. In order to minimize the damage to the underlying superconducting YBCO, caused by exposure to ion milling, the process is performed at an energy lower than that common to bulk etching processes.

In order to evaluate the effects of low-energy blanket ion milling on YBCO films, the electrical properties of critical current density (J_c) and critical temperature (T_c) were measured prior to processing and after repeated exposures. The effects on the structural properties of YBCO were determined using atomic force microscopy (AFM) by which the surface structure was observed for changes and the surface roughness was calculated for a 100 μm^2 area.

Although bulk etching is generally performed at energies greater than 1000 eV and a current density of approximately 1 mA/cm^2, in this work milling steps of 2-minute duration were performed at a beam energy of 500 eV and a beam current density of 0.3 mA/cm^2 in order to minimize residual damage from the ion bombardment. The ion source was oriented normal to the sample surface at a distance of 15 cm. Argon gas was used to create the inert ions. The background pressure during milling was $1x10^{-4}$ Torr. The etch rate of YBCO for these etching parameters was approximately 100 Å/min, so about 200 Å were removed per 2-minute exposure. The initial thickness of the films was approximately 3000 - 4000 Å.

YBCO films were deposited by sputtering or laser ablation on yttria-stabilized zirconia (YSZ), lanthanum aluminate ($LaAlO_3$, or LAO), or strontium titanate ($SrTiO_3$, or STO) substrates. Measurements of J_c and T_c were performed using a non-contact system that employs a current induction technique [10]. AFM data was obtained with a Digital Instruments Dimension 3000 Scanning Probe Microscope. The ion milling was performed with an Ion Tech model FC3000 filament-type 3 cm ion source.

EXPERIMENTAL RESULTS

As previously noted, the intent of the surface preparation process is to remove the non-superconducting surface from YBCO without degrading its electrical or structural properties. However, what has been discovered is an improvement of J_c in some cases and typically a degradation of T_c. Figure 3 shows the plot of T_c for a YBCO film deposited by laser ablation onto a LAO substrate. As can be seen, the onset temperature remains the same while the zero temperature has degraded from 88 K to 83 K after one exposure to the blanket ion milling. Figure 4 shows a plot of critical current (I_c) for the same sample. For a crossover criterion of 20 V, I_c has increased from 11 mA to 25 mA, which corresponds to a J_c increase from $3.77x10^5$ A/cm^2 to $8.57x10^5$ A/cm^2.

Figures 5 and 6 show the T_c and I_c, respectively, of a YBCO film deposited by sputtering onto a YSZ substrate. After one exposure to blanket ion milling, T_c remained

unchanged at 88 K while I_c increased from 30 mA to 36 mA, which corresponds to a J_c increase from 1.029×10^6 A/cm^2 to 1.234×10^6 A/cm^2. Figures 7 and 8 show the T_c and I_c, respectively, of another YBCO film deposited by sputtering on YSZ. After milling, the T_c remained unchanged at 87 K while the I_c increased from 32 mA to 52 mA, which corresponds to a J_c increase from 1.097×10^6 A/cm^2 to 1.783×10^6 A/cm^2.

Not all samples exposed to blanket ion milling behaved in this manner. Figure 9 plots the variation in I_c after each blanket mill for six samples. After one exposure to blanket ion milling, three of the films showed an increase in J_c, two showed a decrease, while one remained unchanged. After the second exposure, one film showed an increase in J_c, three showed a decrease, while one remained unchanged. One sample was milled three times and showed a continous decrease in J_c.

In addition to the electrical properties of YBCO, it is desirable that the surface roughness of the films not be degraded by the in-situ processing to promote epitaxy and planarity. Figure 10 plots the variation in RMS surface roughness (R_q) after each blanket mill for six samples. After one exposure to the blanket ion milling, three of the films showed a decrease in R_q, while three showed an increase. The films consistently showed an increase in R_q after subsequent exposures.

CONCLUSIONS

As discussed previously, the intent of the in-situ surface conditioning process described in this paper is to remove a non-superconducting surface without degrading the electrical or structural properties of YBCO. It has been shown that, in many cases, the J_c of YBCO films can be increased by a 2-minute exposure to an argon ion beam at 500 eV and 0.3 mA/cm^2. The increase in J_c is believed to be due to damage caused by the argon ions which creates flux pinning centers on the surface of the YBCO [11,12].

The effect on surface roughness of low-energy blanket ion milling are intriguing. While the films studied here showed some increase in surface roughness, the amount of the increase is acceptable considering that these films initially are sufficiently smooth for patterning of lines as small as 5 μm. It has also been found that films with poor initial roughness (>30 nm RMS) are consistently smoothed by low-energy blanket ion milling. The films that did show an increase in roughness initially contained many pits on the surface which were progressively worsened by the milling. Films which were initially pit-free were shown to decrease in roughness after milling, even for films which were initially very smooth (<10 nm RMS).

The effects of ion milling on the electrical properties of YBCO films correlate well with changes in roughness. Films which exhibited high quality initially were more likely to be improved by low-energy blanket ion milling. On the other hand, poorer quality films typically degraded with ion milling. However, the results of these experiments show that YBCO films can be exposed to low-energy blanket ion milling

with relatively little detrimental effect on their electrical or structural properties. In fact, it may be reasonable to perform ion milling with the intent of increasing the J_c of YBCO films.

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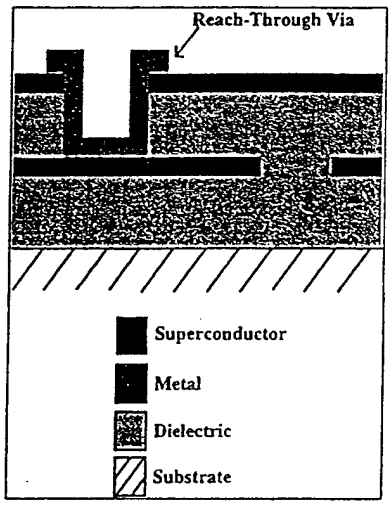

Figure 1: Interconnect Structure

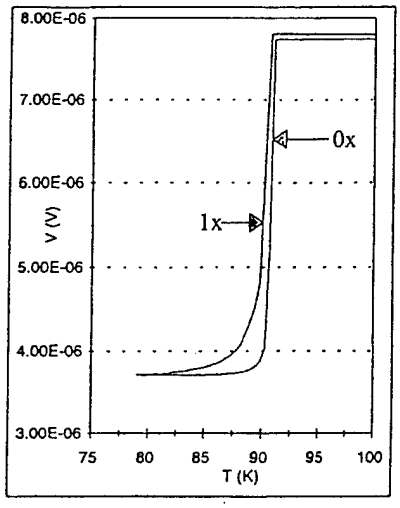

Figure 3: T_c of laser-deposited YBCO on LAO

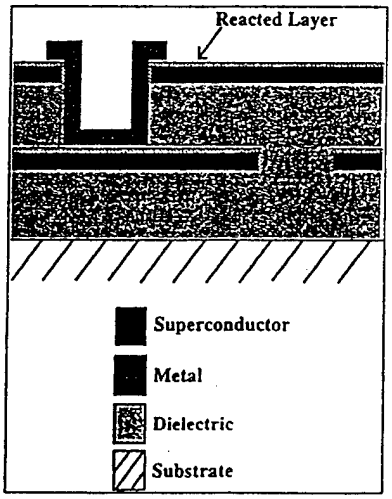

Figure 2: Reactivity of YBCO

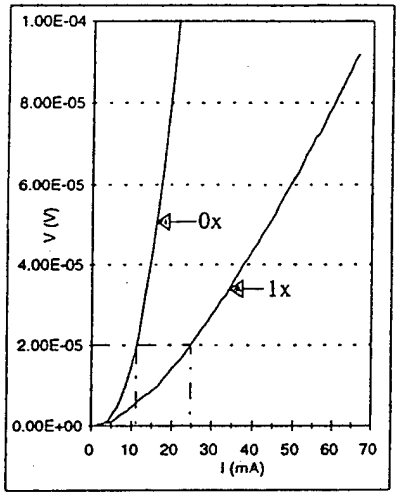

Figure 4: I_c of laser-deposited YBCO on LAO

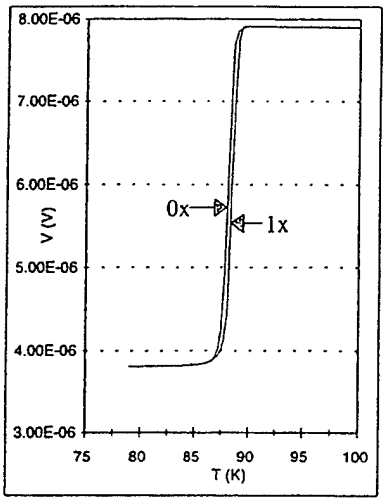

Figure 5: T_c of sputtered YBCO on YSZ

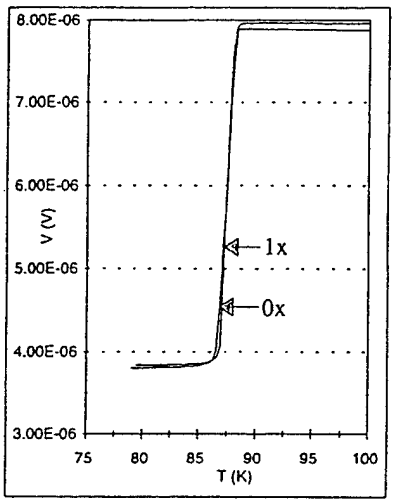

Figure 7: T_c of sputtered YBCO on YSZ

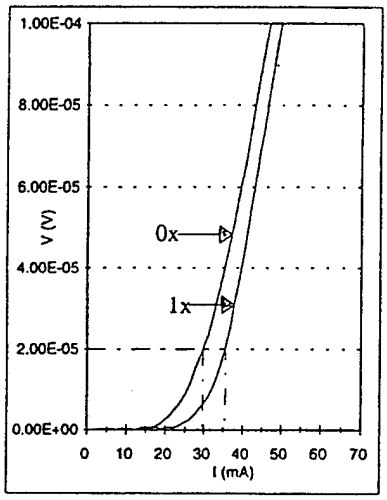

Figure 6: I_c of sputtered YBCO on YSZ

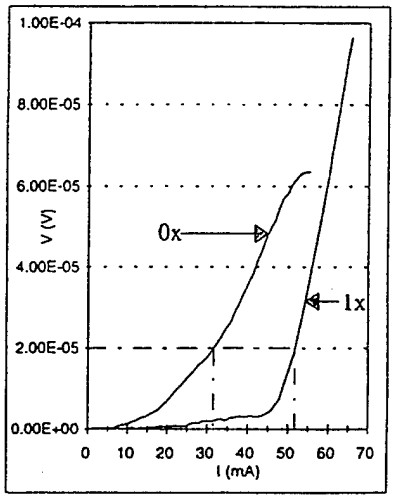

Figure 8: I_c of sputtered YBCO on YSZ

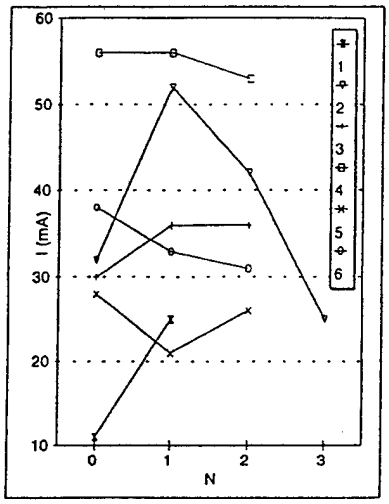

Figure 9: I_C vs. number of mills

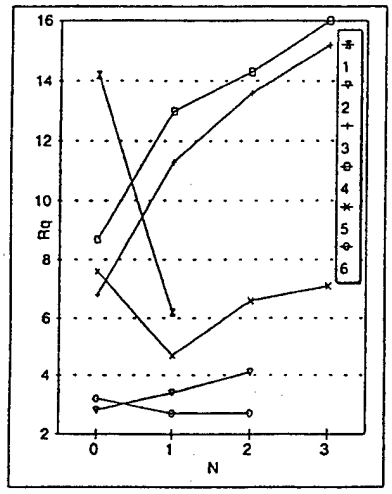

Figure 10: RMS roughness vs. number of mills

PROCEEDINGS OF THE SYMPOSIUM ON

LOW TEMPERATURE ELECTRONICS AND HIGH TEMPERATURE SUPERCONDUCTIVITY

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Ion Beam Assisted Sputter Deposition of CeO_2 Buffer Layers for Superconducting Multichip Module (MCM) Applications

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Cerium dioxide (CeO_2) buffer layers have been sputter deposited onto various substrates including silicon and nickel alloy using ion beam assisted deposition (IBAD). This technique has resulted in the formation of CeO_2 which exhibits strong (100) phase growth as well as in-plane orientation as evidenced by X-ray diffraction. Subsequent YBCO depositions on these films exhibit T_c's of 86 K and biaxial texture with the c-axis normal to the surface. With further refinement, this technique may be used to fabricate the multilayer structure needed for superconducting multichip modules.

INTRODUCTION

There is widespread interest in the use of superconducting interconnects in electronics, especially in multichip modules (MCMs). Superconductor interconnects have advantages of low signal loss and very low RC propagation delays. Furthermore, due to the reduction in interconnect resistance, the linewidths can be made much smaller, allowing for a reduction in the number of signal layers. One proposed structure for the superconducting MCM is the interconnected mesh power system (IMPS), which requires only two interconnect layers, thereby reducing the complexity of the manufacturing process (1). In order to achieve satisfactory electrical performance and reduce parasitic capacitances, these interconnects need to be separated by a thick (~2-5 μm) insulating layer with a low dielectric constant. Possible substrate and dielectric materials for these applications include silicon, silicon dioxide, or other polycrystalline materials. However, it has been shown that YBCO deposited directly onto these materials reacts with them and degrades the YBCO superconducting properties. The use of buffer layers such as cerium dioxide (CeO_2) or yttria-stabilized zirconia (YSZ) can mitigate these problems, but they have high dielectric constants and need to exhibit a high degree of biaxial texture to reduce high-angle grain boundaries and improve the critical current density, J_c, of the YBCO layer.

One possible interconnect structure that has been proposed by researchers at the High Density Electronics Center (HiDEC) consists of two YBCO layers separated by a thick layer of SiO_2, which exhibits a low dielectric constant. To prevent interdiffusion and provide for an epitaxial surface on which high quality YBCO can be deposited, the SiO_2 is

see presentation at

separated from the YBCO by a thin buffer layer of either cerium dioxide or yttria-stabilized zirconia. Clearly, the ability to deposit aligned buffer layers on polycrystalline or amorphous substrates would greatly improve the manufacturability of superconducting MCMs.

Ion beams have been used previously to deposit aligned buffer layers for YBCO on polycrystalline substrates. Iijima *et al.* (2) reported a dual-ion beam process for depositing YSZ on Hastelloy C276, a nickel-based alloy. The ion beam position with respect to the substrate normal was varied from 30° to 60°, with bi-axially oriented films obtained at an angle of 45°. Reade *et al.* (3) also reported biaxial deposition of YSZ on nickel alloys when using ion beam assisted deposition in conjunction with laser ablation. The degree of orientation of the films was found to be strongly dependent on the incident angle of the ion beam, with the optimal results occurring at 55° from the substrate normal. Ion beam voltage and current also played important roles in determining the amount of orientation of the film. Oriented YSZ growth on Pyrex substrates using IBAD has also been reported by Sonnenberg *et al* (4). They reported detailed microstructural characterization, but did not subsequently deposit YBCO on these films. This paper reports our progress to date in the use of IBAD with magnetron sputtering, which has the advantage of producing larger area films than laser ablation.

EXPERIMENTAL DETAILS

All of the buffer layer films were deposited by RF magnetron sputtering in a deposition system designed at the University of Arkansas for superconductor and related dielectric research. Briefly, it is a 22" diameter side-sputtering deposition system that is pumped with two cryopumps. The deposition pressure can be precisely controlled from high vacuum to above 1 Torr, independently of the amount of backfill gas present. This is achieved through the use of separate high- and low-conductance paths to the cryopumps. Both conductance paths utilize servo-controlled throttle valves to maintain a constant pressure regardless of the gas flow present. The chamber has multiple ports for mounting two sputter guns, an ion beam, and two substrate holders, which also serve as heaters. The chamber was pumped down to 4×10^{-7} Torr before each deposition.

The ion beam used in these experiments is an Anatech IS-3000 3" filamentless gun. It was positioned about 8 cm from the substrate and at an angle of 55° from the substrate normal. This corresponds to the angle of the [111] direction from the [100] direction for cubic CeO_2, and it is believed that ions directed at this angle may suppress growth of the (111) phase while enhancing growth of the (100) phase (3). Argon gas was flowed through the gun and an acceleration potential of 200-300 eV was used, with a beam current of 2-5 mA.

The dielectric films were deposited from a stoichiometric 2" diameter CeO_2 target which was RF sputtered in 80% Ar and 20% O_2 at pressures ranging from 0.2 mTorr to 1 mTorr, and at power levels from 60-80 watts. The low pressures were required to create

a long enough mean free path for the ion gun to maintain a collimated beam. According to basic vacuum theory, a mean free path of 8 cm requires a pressure lower than 0.61 mTorr. Special modifications were made to the sputtering guns to allow them to maintain plasmas at such low pressures. These modifications basically consisted of flowing the sputtering gas inside the dark space shield of the sputter guns, creating a localized high pressure region. The substrate was unheated, but its temperature generally increased to about 50 °C due to radiative heating from sputtering and the ion beam.

The YBCO films were deposited in the same system described above, using a 2" magnetron sputtering gun in an off-axis geometry; the parameters are described elsewhere (5). Briefly, substrates were mounted onto a heater block using silver paste. The deposition temperature was held at 735 °C in 80% Ar and 20% O_2. After deposition, the samples were cooled in 700 Torr of oxygen.

The following substrates were used in this experiment: pieces of <100> prime silicon, 1" square Corning 7059 borosilicate glass (Pyrex), and 0.5" square Haynes alloy (#230). Haynes alloy is a nickel-based stainless steel which is a candidate substrate for YBCO films because of its low thermal expansion coefficient mismatch with YBCO. The Haynes alloy was mechanically polished using successively finer diamond paste to 0.25 μm. The three different materials represent crystalline, amorphous, and polycrystalline structures, respectively, and provide a thorough test of the ability of IBAD to deposit oriented films independently of the substrate structure or orientation.

Cerium dioxide films were deposited on the above substrates both with and without IBAD. All of the films in this study were grown to a thickness of about 2000 Å. The use of IBAD caused a decrease in the deposition rate, from about 16 Å/min to 13 Å/min. After all of the CeO_2 depositions were completed, the CeO_2 sputtering gun was removed and replaced with the YBCO sputtering gun. The CeO_2 films were removed for analysis, then remounted to the heater block for YBCO deposition. YBCO films of approximately 3500 Å thickness were deposited on the glass and Haynes substrates.

The thickness and index of refraction of the CeO_2 films deposited on bare silicon were measured using an ellipsometer. The structure of the films was analyzed with a Phillips PW-1830 four-circle x-ray diffractometer (XRD) using copper kα radiation, and the surface analysis was performed with a Digital Instruments atomic force microscope (AFM). Electrical characteristics were measured using a non-contact technique similar to the system described in (6).

RESULTS AND DISCUSSION

The index of refraction of both the IBAD and non-IBAD films was around 2.3, compared to 2.2 for bulk CeO_2. This indicates that the films are slightly oxygen deficient (7), but theta-two theta XRD scans show only evidence of the CeO_2 phase. The theta-two theta scan of CeO_2 on a silicon substrate without using IBAD is shown in figure 1. The presence of the (111), (200), and the (220) peaks are present at roughly the same

intensity, with the ratio of the (200) peak intensity to (111) peak intensity equal to 0.95. This suggests a polycrystalline film with no prevalent texture. The film consists of completely random oriented grains since the substrate does not provide epitaxy for the growing layers. Figure 2 shows the theta-two theta scan of CeO_2 on silicon using IBAD. As the figure indicates, IBAD causes a marked improvement in the texturing of the (100) phase. The other phases are significantly attenuated, with the ratio of (200) to (111) intensities equal to 14.5. One reason for this dramatic improvement in texture, besides the fact that IBAD was used, is that silicon is crystalline with very nearly the same lattice constant as CeO_2.

Figure 3 shows a theta-two theta XRD scan of IBAD deposited CeO_2 on Pyrex. While the (111) and (220) peaks are still visible, the (200) peak is dominant; the ratio of (200) to (111) intensities is 1.4. Figure 4 shows a phi scan of the (111) family of CeO_2 peaks on Pyrex and indicates both in-plane and out-of-plane orientation, as evidenced by the four peaks spaced 90° apart. The full-width-at-half-maximum (FWHM) for these peaks is approximately 34°. The relatively high FWHM implies that some in-plane misorientation is present. A theta-two theta scan of YBCO/CeO_2/Pyrex is presented in figure 5. Only c-axis YBCO growth is detected, which suggests that the CeO_2 deposition provides a well-aligned layer upon which the YBCO can be deposited. As a further demonstration of the alignment, figure 6 shows a phi scan of the YBCO (103) family of peaks with a FWHM of 22°. This indicates well-aligned grains in the a-b plane, which is parallel to the substrate. The presence of 45° misaligned grains would be indicated by peaks spaced 45° out of phase from the major peaks. Misaligned grains greatly reduce the J_c of the films.

Next, data for CeO_2 and YBCO/CeO_2 structures deposited on Haynes alloy are presented. Figure 7 shows a theta-two theta scan for CeO_2 deposited without IBAD. In this case, the CeO_2 peaks are barely discernible above the noise of the substrate, with the (111), (200), and (220) peaks at about equal intensity. The ratio of (200) to (111) intensities is equal to 0.9. Figure 8 illustrates a theta-two theta scan of YBCO deposited on Haynes alloy with an IBAD-deposited CeO_2 buffer layer. As in figure 5, only c-axis YBCO growth is evident. In addition, the (200) peak of CeO_2 is 3.2 times more intense than the (111) peak.

YBCO was deposited on the three CeO_2/substrate structures and their T_cs and J_cs were measured. T_cs (zero resistance) were 86 K, and J_cs ranged from 1×10^5 A/cm^2 to 5×10^5 A/cm^2 when measured at 77 K. These values are somewhat lower than T_cs and J_cs obtained for films deposited on single crystal substrates, such as yttria stabilized zirconia. The cause for the reduction in J_c is most likely due to the presence of high-angle grain boundaries, which are evident from the scan shown in figure 6. These grain boundaries are known to act as weak links and reduce the critical current density (8).

It is not well understood how the ion beam provides oriented film growth, but three separate mechanisms have been postulated. First, the collimated ion beam may selectively sputter grains growing in undesirable directions. Second, the beam is believed

to enhance film growth corresponding to the channeling direction of the film. As mentioned above, the [111] channeling direction is 55° away from the [100] direction. Therefore, a beam directed at this angle allows the (100) phase to become channeled to the growing film, while other phase growth is attenuated or slowly sputtered away. Finally, the ion beam imparts energy to the surface of the film, which provides increased mobility for the molecules to realign into the preferred orientation.

The average roughness R_a of the IBAD films was measured by AFM and found to be about 2.6 nm, while the R_a of the non-IBAD films was about 3.8 nm. This improvement in smoothness is most likely due to the tendency of the ion beam to etch peaked surfaces more rapidly than smooth areas (9). This enhances superconductor quality by providing a smooth surface for YBCO nucleation. The improved surface quality, along with the stronger presence of the (100) phase, is believed to be responsible for higher YBCO film quality.

CONCLUSIONS

Cerium dioxide films have been sputter deposited onto several substrate materials using IBAD. These films exhibit bi-axial alignment with dominant (100) phase growth, as indicated by XRD theta-two theta and phi scans. The argon ion beam was positioned 55° from the substrate normal. This angle corresponds to the angle of separation of the [111] direction of cubic CeO_2 from the [100] direction.

High quality YBCO was deposited over the IBAD buffer layers The YBCO exhibited T_cs around 86 K and J_cs ranging from 1×10^5 A/cm^2 to 5×10^5 A/cm^2. IBAD has been shown to be a useful technique for depositing aligned films on crystalline, polycrystalline, and amorphous substrates. This capability allows greater flexibility in manufacturing superconductor-dielectric structures by enabling the use of low-cost substrates in place of lattice-matched single crystal substrates, which tend to be expensive, brittle, and have high dielectric constants.

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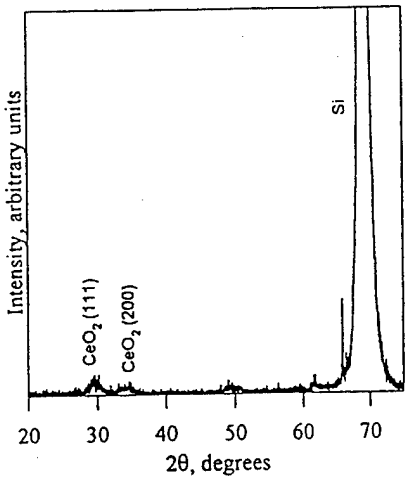

Figure 1. XRD scan of CeO_2 deposited on Si without IBAD.

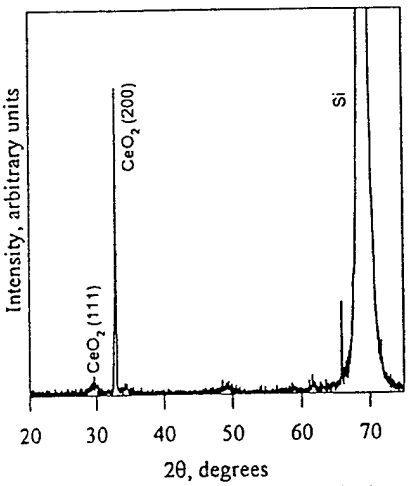

Figure 2. XRD scan of CeO_2 deposited on Si with IBAD.

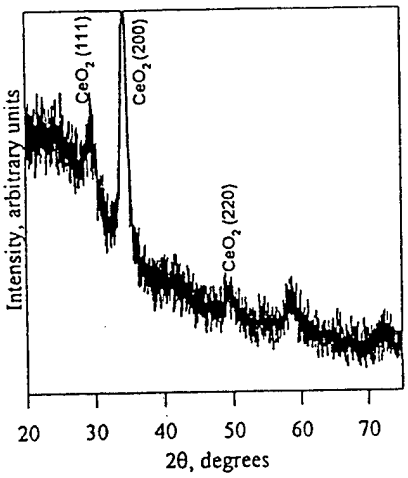

Figure 3. XRD scan of CeO_2 deposited on Pyrex with IBAD.

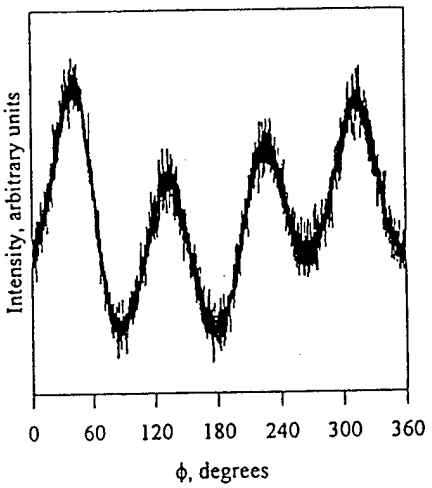

Figure 4. Phi scan of $CeO2_2$ (111) family of peaks deposited on Pyrex.

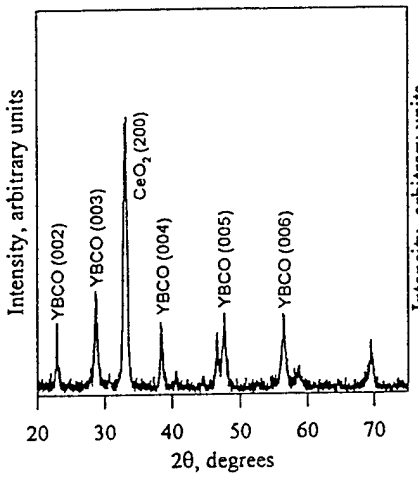

Figure 5. XRD scan of YBCO/CeO_2 deposited on Pyrex with IBAD.

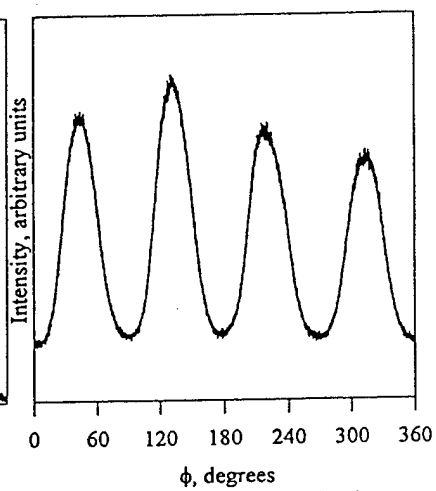

Figure 6. Phi scan of YBCO (103) family of peaks on CeO_2/Pyrex.

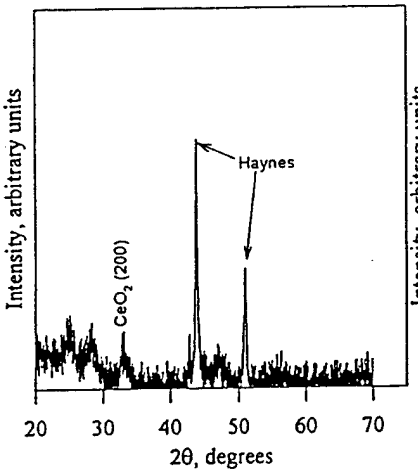

Figure 7. XRD scan of CeO_2 deposited on Haynes without IBAD.

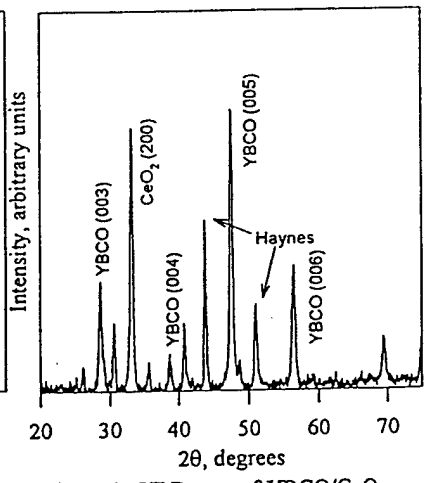

Figure 8. XRD scan of YBCO/CeO_2 deposited on Haynes with IBAD.

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Ion-beam-assisted sputter deposition of YSZ buffer layers for superconducting interconnect applications

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Received 1 March 1995, in final form 19 April 1995

Abstract. Yttria-stabilized zirconia (YSZ) buffer layers have been sputter deposited onto various substrates including silicon and nickel alloy using ion-beam-assisted deposition (IBAD). This technique resulted in the formation of buffer layers which exhibit strong (100) phase growth as well as in-plane orientation as evidenced by x-ray diffraction measurements. Subsequent YBCO depositions on these films exhibit T_c values of 86 K and strong biaxial texture with the *c* axis normal to the surface. With further refinement, this technique may be used to fabricate the multilayer substrate structure needed for superconducting multichip modules.

1. Introduction

There is widespread interest in the use of superconducting interconnects in electronics, especially in multichip modules (MCMs). Interconnects made of superconducting material have the advantage of low signal loss and very low *RC* propagation delays. Furthermore, due to the reduction in interconnect resistance, the linewidths can be made much smaller, allowing for higher density circuitry. Superconducting MCMs require both large-area substrates and thick dielectrics in order to become technologically viable. Large area single-crystal materials such as magnesium oxide (MgO), yttria-stabilized zirconia (YSZ), and lanthanum aluminate ($LaAlO_3$) are difficult and expensive to produce. Furthermore, these materials have very high dielectric constants, which makes them unsuitable for separating interconnect layers. In order to achieve satisfactory electrical performance and reduce parasitic capacitances at high signal speeds, these interconnects need to be separated by a thick (approximately 2–5 μm) insulating layer with a low dielectric constant. Possible substrate and dielectric materials for these applications include silicon, silicon dioxide, or other polycrystalline materials. However, it is widely known that YBCO deposited directly onto these materials reacts with them and degrades the YBCO superconducting properties. The use of buffer layers, such as cerium dioxide (CeO_2) or YSZ, reduces substrate–YBCO interaction problems, but these materials have high dielectric constants and need to exhibit a high degree of biaxial texture to reduce high-angle grain boundaries and improve the critical current density, J_c, of the YBCO layer.

One possible interconnect structure that has been proposed by researchers at the High Density Electronics Center (HiDEC) consists of two YBCO layers separated by a thick layer of SiO_2, which exhibits a low dielectric constant. To prevent interdiffusion and provide for an epitaxial surface on which high-quality YBCO can be deposited, the SiO_2 is separated from the YBCO by a thin buffer layer of either CeO_2 or YSZ. Clearly, the ability to deposit aligned buffer layers on large polycrystalline or amorphous substrates would greatly improve the manufacturability and feasibility of superconducting MCMs.

Ion beams have been used previously to deposit aligned buffer layers for YBCO on polycrystalline substrates. Iijima *et al* [1] reported a dual-ion beam process for depositing YSZ on Hastelloy C276, a nickel-based alloy. The ion beam position with respect to the substrate normal was varied from 30° to 60°, with biaxially oriented films obtained at an angle of 45°. The energy of the ion beam was varied from 300 eV to 1000 eV, with best results obtained for energies less than 700 eV. Subsequent YBCO depositions over these films resulted in J_c values of 2.5×10^5 A cm^{-2} at 77 K.

Reade *et al* [2] also reported deposition of biaxial YSZ on nickel alloys when using ion-beam-assisted deposition (IBAD) in conjunction with laser ablation. The degree of orientation of the films was found to be strongly dependent on the incident angle of the ion beam, with

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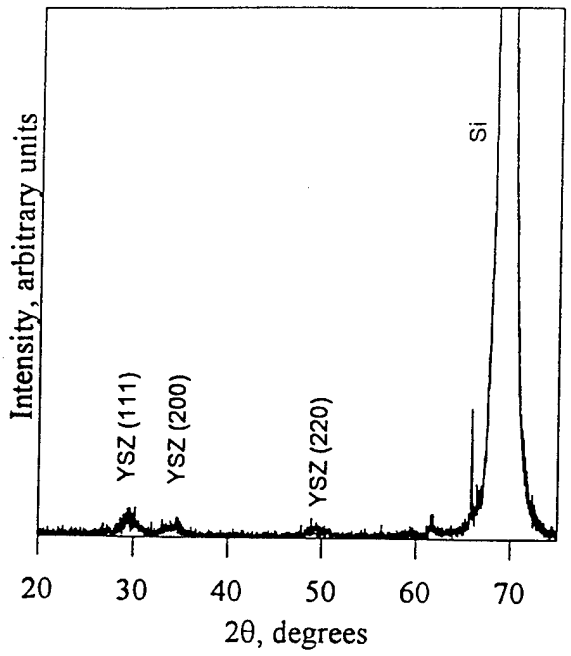

Figure 1. XRD scan of YSZ deposited on Si substrate without IBAD.

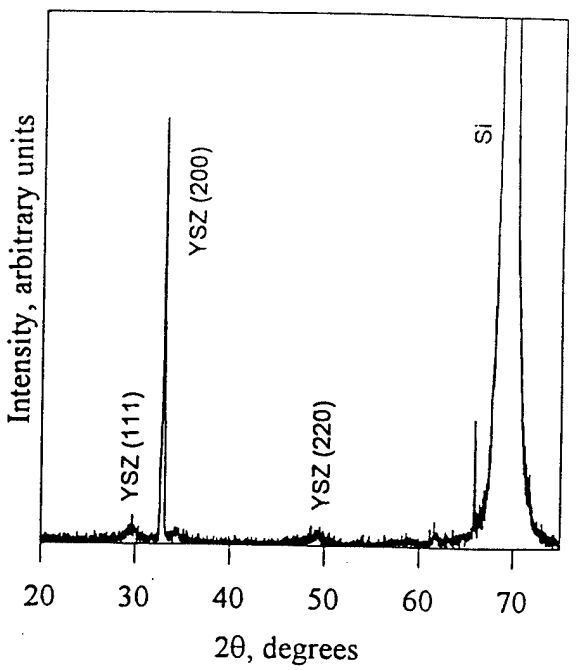

Figure 2. XRD scan of YSZ deposited on Si substrate with IBAD.

the optimal results occurring at 55° from the substrate normal. Ion beam voltage also played an important role in determining the amount of orientation of the film. They found that higher beam voltages increased film texture, whereas voltages less than 50 V resulted in films with no apparent *a–b* plane orientation. Changing the beam current did not enhance film texture, and currents above 50 mA reduced film deposition rates. The use of oxygen in the ion beam resulted in (100) film orientation, but no in-plane texture was observed. YBCO deposited on the oriented films exhibited T_c values of 92 K and J_c values of 6×10^5 A cm^{-2}.

Recently, Wu *et al* [3] reported CeO_2/YSZ layers deposited on flexible nickel substrates using IBAD and laser ablation. The thickness of the YSZ was 6000 to 8000 Å. A 1000 Å layer of CeO_2 was then deposited over the YSZ in order to better match the lattice constants of YBCO. The full width at half-maxima (FWHM) of the (220) peaks of YSZ were found to be 14–15°. YBCO films deposited over the buffer layers exhibited J_c values of 8×10^5 A cm^{-2}, and the FWHM of the (103) peaks were about 10°.

Oriented YSZ growth on Pyrex substrates using IBAD in conjunction with electron beam evaporation has also been reported by Sonnenberg *et al* [4]. They reported detailed microstructural characterization, but did not subsequently deposit YBCO on these films. ϕ scans of the films revealed strong orientation in the *a–b* plane. This was indicated by the presence of (111) peaks spaced 90° apart. Films were held at various angles from the ion beam, and (100) orientation was noted from 25° to 63° [4] from substrate normal, with 48° yielding the highest degree of orientation.

In the above studies, the substrate sizes were 18 mm by 10 mm, 10 mm square, or 5 mm square. The use of superconductor interconnects in MCMs will require large-area films, and these are difficult to obtain with laser ablation. This paper reports our progress to date on the use of IBAD with magnetron sputtering, which has the advantage of being able to produce films approximately the same size as the sputtering target. However, IBAD is more difficult to implement in sputtering systems because of the low pressures (10^{-6} to 10^{-4} Torr) that ion beams require to operate. Furthermore, glow discharges are difficult to maintain at these pressures, especially in the presence of oxygen.

2. Experimental details

All of the buffer layer films were deposited by RF magnetron sputtering in a deposition system designed at the University of Arkansas for superconductor and related dielectric research. Briefly, it is a 22″ diameter side-sputtering deposition system that is pumped with two cryopumps. The deposition pressure can be precisely controlled from high vacuum to above 1 Torr, independently of the flow levels of backfill gas. This is achieved through the use of separate high- and low-conductance paths to the cryopumps. Both conductance paths utilize servo-controlled throttle valves to maintain a constant pressure regardless of the gas flow present. The chamber has multiple ports for mounting two sputter guns, an ion beam, and two substrate holders, which also serve as heaters. The chamber was pumped down to 3×10^{-7} Torr before each deposition to ensure adequate removal of water vapour.

The ion beam used in these experiments is an Anatech IS-3000 3″ filamentless gun. It was positioned about 8 cm from the substrate and at an angle of 55° from the substrate normal. This corresponds to the angle of the [111] direction from the [100] direction for cubic YSZ, and it is believed that ions directed at this angle may suppress growth of the (111) phase while enhancing growth of the (100) phase [2]. Argon gas was flowed through the gun at a rate of 30 sccm,

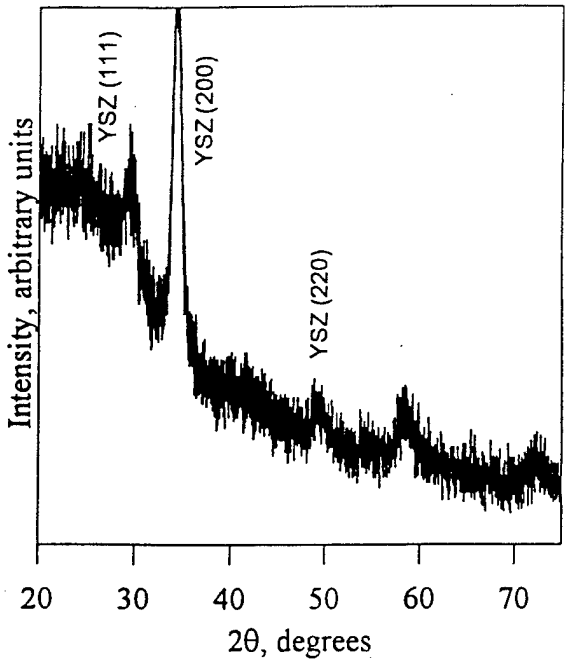

Figure 3. XRD scan of YSZ deposited on Pyrex substrate with IBAD.

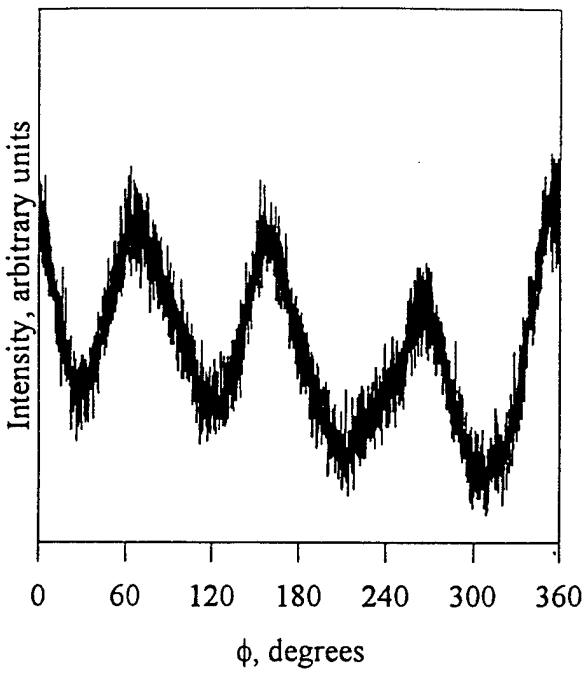

Figure 4. ϕ scan of YSZ (111) family of peaks for the film shown in figure 3.

ınd an acceleration potential of 200–300 eV was used, with ı beam current of 2–5 mA.

The dielectric films were deposited from a 3″ diameter YSZ target (8% by weight yttria) using a Torus 3C nagnetron sputtering gun. The target was RF sputtered n a mixture of 16 sccm Ar and 4 sccm O_2 at a pressure of).5 mTorr, and at power levels from 160–200 watts. The ow pressures were required to create a sufficiently long nean free path for the ion gun to maintain a collimated)eam. According to basic vacuum theory, a mean free path)f 8 cm requires a pressure lower than about 0.6 mTorr.)pecial modifications were made to the sputtering guns o allow them to maintain plasmas at such low pressures. These modifications basically consisted of flowing the puttering gas inside the dark space shield of the sputter guns, creating a localized high pressure region. This, in conjunction with the magnetron field, confined the plasma o a region very near the surface of the target. The substrate vas not intentionally heated, but its temperature generally ncreased to about 100 °C due to radiative heating from puttering and the ion beam. The YBCO films were leposited in the same system described above, using a ″ magnetron sputtering gun in an off-axis geometry; the)arameters are described elsewhere [5]. Briefly, substrates vere mounted onto a heater block using silver paste. The leposition temperature was held at 735 °C in 90% Ar and 0% O_2. After deposition, the samples were cooled in 700 Torr of oxygen.

The following substrates were used in this experiment:)ieces of ⟨100⟩ prime silicon, 1″ square Corning 7059)orosilicate glass (Pyrex), and 0.5″ square Haynes alloy No 230). Haynes alloy is a nickel-based stainless steel which is a candidate substrate for YBCO films because of ts low thermal expansion coefficient mismatch with respect o YBCO. The Haynes alloy was mechanically polished ısing successively finer diamond paste to 0.25 μm. The three different materials represent crystalline, amorphous, and polycrystalline structures, respectively, and provide a thorough test of the ability of IBAD to deposit oriented films independent of the substrate structure or orientation. YSZ films were deposited on the above substrates both with and without IBAD. All of the films in this study were grown to a thickness of about 2000 Å. The use of IBAD caused a decrease in the deposition rate, from about 40 Å min^{-1} to 33 Å min^{-1}. After all of the YSZ depositions were completed, the YSZ sputtering gun was removed and replaced with the YBCO sputtering gun. The YSZ films were removed for analysis, then remounted to the heater block for YBCO deposition. YBCO films of approximately 3500 Å thickness were deposited on the glass and Haynes substrates.

The thickness and index of refraction of the YSZ films deposited on bare silicon were measured using an ellipsometer. The structure and orientation of the films were analysed with a Phillips PW-1830 four-circle x-ray diffractometer (XRD) using Cu Kα radiation, and the surface analysis was performed with a Digital Instruments atomic force microscope (AFM). Electrical characteristics were measured using a non-contact technique similar to the system described in [6]. Basically the system consists of a small coil of wire placed near the YBCO film. The coil-film assembly is cooled, and the coil is driven with a 10 kHz signal. As the film makes the transition from the normal state to the superconducting state, the inductance drops substantially due to shielding currents that are induced in the film. The T_c is obtained by noting the temperature at which a significant reduction in reflected voltage occurs. The J_c is obtained by increasing the drive current of the coil while held at 77 K. Eventually, harmonic voltages will appear in the coil, which indicate the onset of normal state resistance. The coil current at which the voltages appear is proportional to J_c.

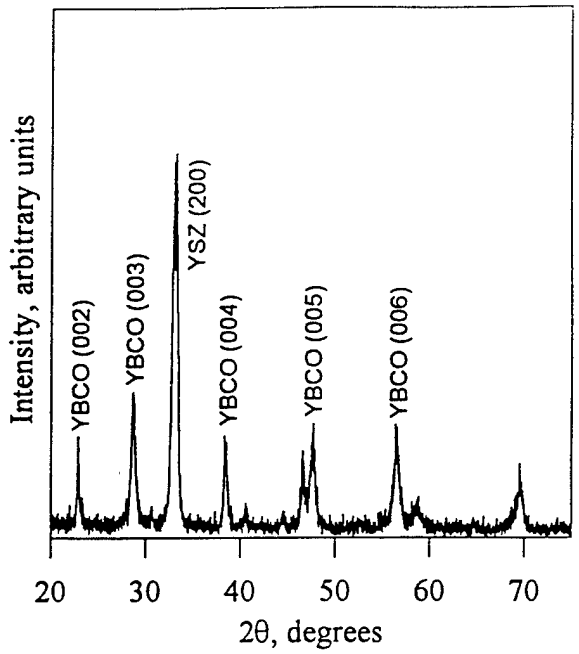

Figure 5. XRD scan of YBCO/YSZ deposited on Pyrex substrate with IBAD.

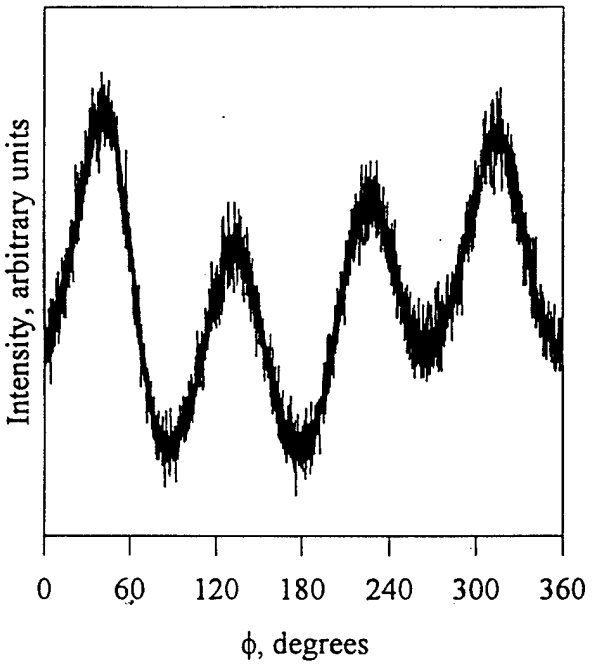

Figure 6. ϕ scan of YSZ (111) family of peaks for the film shown in figure 5.

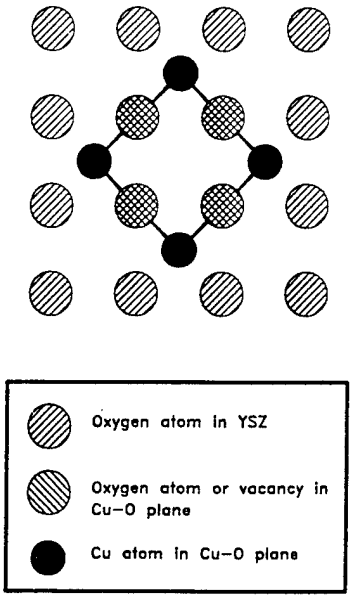

Figure 7. Illustration of the 45° (alignment of *c*-axis oriented YBCO on (100) oriented YSZ.

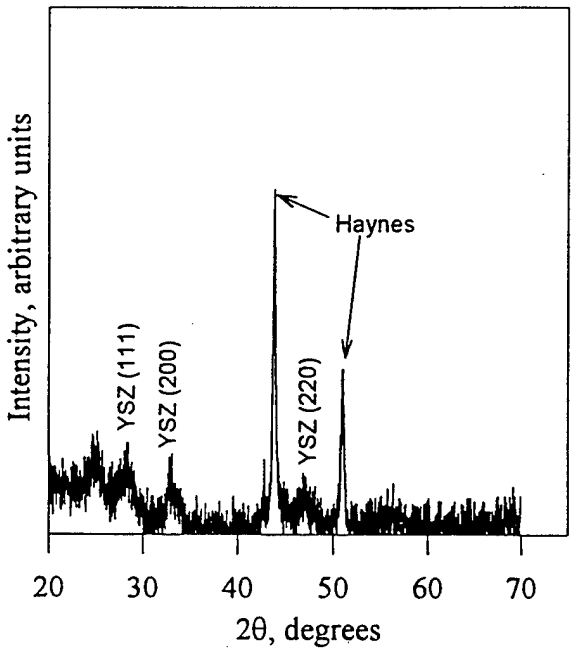

Figure 8. XRD scan of YSZ deposited on Haynes alloy substrate without IBAD.

3. Results and discussion

The θ–2θ scan of YSZ on a silicon substrate without using IBAD is shown in figure 1. The (111), (200) and the (220) peaks are present at roughly the same intensity, with the ratio of the (200) peak intensity to (111) peak intensity equal to 0.9. This indicates a polycrystalline film with no prevalent texture. The film consists of completely random oriented grains since the substrate does not provide epitaxy for the growing layers. Figure 2 shows the θ–2θ scan of YSZ on silicon using IBAD. As the figure indicates, IBAD causes a marked improvement in the texturing of the (h00) phase. The other phases are significantly attenuated, with the ratio of (200) to (111) intensities equal to 15. One reason for this dramatic improvement in texture, besides the fact that IBAD was used, is that silicon is crystalline with very nearly the same lattice constant as YSZ.

Figure 3 shows a θ–2θ XRD scan of IBAD deposited YSZ on Pyrex. While the (111) and (220) peaks are still visible, the (200) peak is dominant; the ratio of (200) to (111) intensities is 1.5. Figure 4 shows a ϕ scan of the (111) family of YSZ peaks on Pyrex and indicates both in-plane and out-of-plane orientation, as evidenced by the four peaks spaced 90° apart. The full width at half-maximum (FWHM) for these peaks is approximately 34°. The relatively high FWHM implies that some in-plane misorientation is present. A θ–2θ scan of YBCO/YSZ/Pyrex is presented

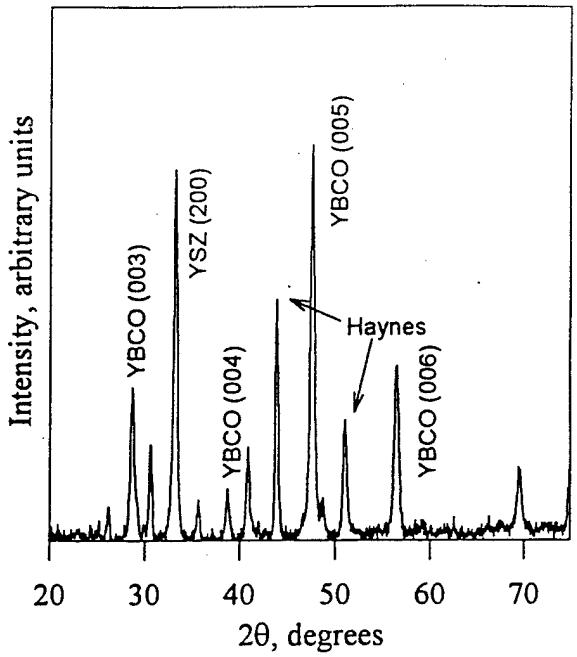

Figure 9. XRD scan of YBCO/YSZ deposited on Haynes alloy substrate with IBAD.

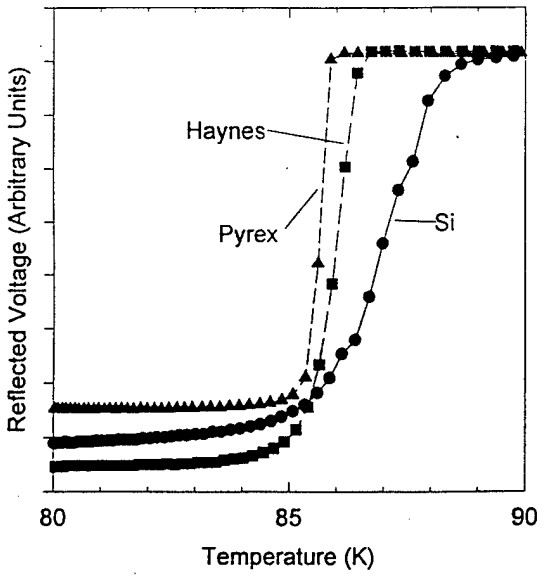

Figure 10. Transition temperature measurements for YBCO deposited on three different substrate materials.

in figure 5. Only *c*-axis YBCO growth is detected, which suggests that the YSZ deposition provides a well-aligned layer upon which the YBCO can be deposited. As a further demonstration of the alignment, figure 6 shows a ϕ scan of the YBCO (103) family of peaks with a FWHM of 22°. This indicates well-aligned grains in the *a*–*b* plane, which is parallel to the substrate. The presence of 45° misaligned grains would be indicated by peaks spaced 45° out of phase from the major peaks. Misaligned grains greatly reduce the J_c of the films [7], and thus, should be minimized. The (103) family of peaks are rotated 45° from the positions of the YSZ peaks shown in figure 4. This is expected since (100) orientations of YBCO tend to align with the CuO plane at a 45° rotation from the oxygen atoms in YSZ, as indicated in figure 7.

Next, data for YSZ and YBCO/YSZ structures deposited on Haynes alloy are presented. Figure 8 shows a θ–2θ scan for YSZ deposited without IBAD. In this case, the YSZ peaks are barely discernible above the noise of the substrate, with the (111), (200) and (220) peaks at about equal intensities. The ratio of (200) to (111) intensities is equal to 0.9. Figure 9 illustrates a θ–2θ scan of YBCO deposited on Haynes alloy with an IBAD-deposited YSZ buffer layer. As in figure 5, only *c*-axis YBCO growth is evident. In addition, the (200) peak of YSZ is 3.2 times more intense than the (111) peak.

YBCO was deposited on each of the three IBAD YSZ/substrate combinations and their T_c and J_c values were measured. T_c values (zero resistance) were 86 K, and J_c values ranged from 2×10^5 A cm^{-2} to 7×10^5 A cm^{-2} when measured at 77 K. Figure 10 shows the T_c plots for the films deposited on the three different substrates. These values are somewhat lower than T_c and J_c values obtained for films deposited on single-crystal YSZ substrates. The cause for the reduction in J_c is most likely due to the presence of high-angle grain boundaries, which are evident from the scan shown in figure 6. These grain boundaries are known to act as weak links and reduce the critical current density [8].

It is not well understood how the ion beam provides oriented film growth, but three separate mechanisms have been postulated. First, the collimated ion beam may selectively sputter grains growing in undesirable directions. Second, the beam is believed to enhance film growth corresponding to the channelling direction of the film. As mentioned above, the [111] channelling direction is 55° away from the [100] direction. Therefore, a beam directed at this angle allows the (100) phase to become channelled to the growing film, while other phase growth is attenuated or slowly sputtered away. Finally, the ion beam imparts energy to the surface of the film, which provides increased mobility for the molecules to realign into the preferred orientation.

The average roughness R_a of the IBAD films was measured by AFM and found to be about 2.7 nm, while the R_a of the non-IBAD films was about 4.5 nm. This improvement in smoothness is most likely due to the tendency of the ion beam to etch peaked surfaces more rapidly than smooth areas, thus reducing RMS roughness [9]. This enhances superconductor quality by providing a smooth surface for YBCO nucleation. The improved surface quality, along with the stronger presence of the (100) phase, is believed to be responsible for higher YBCO film quality.

4. Conclusions

Yttria-stabilized zirconia films have been sputter deposited onto several substrate materials using IBAD. These films exhibit biaxial alignment with dominant (100) phase growth, as indicated by XRD θ–2θ and ϕ scans. The argon ion beam was positioned 55° from the substrate normal. This angle corresponds to the angle of separation of the [111] direction of cubic YSZ from the [100] direction.

High-quality YBCO was sputter deposited over the IBAD YSZ buffer layers. The YBCO exhibited T_c values around 86 K and J_c values ranging from 2×10^5 A cm^{-2} to 7×10^5 A cm^{-2}. IBAD has been shown to be a useful technique for depositing aligned films on crystalline, polycrystalline, and amorphous substrates. This capability allows greater flexibility in manufacturing superconductor–dielectric structures by enabling the use of low-cost substrates in place of lattice-matched single-crystal substrates, which tend to be expensive, brittle, and have high dielectric constants.

Acknowledgments

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Sputter-deposited yttrium–barium–copper–oxide multilayer structures incorporating a thick interlayer dielectric material

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Physical vapor deposition technologies have been developed which allow the fabrication of multilayer structures consisting of two yttrium–barium–copper–oxide ($YBa_2Cu_3O_{7-x}$ or YBCO) layers separated by a thick (~4 μm), low dielectric constant material. The YBCO is buffered from both the substrate and the other films with ion-beam assisted deposited (IBAD) films of yttria-stabilized zirconia (YSZ). The YSZ layer provides both the texture necessary to deposit high-quality YBCO films and protection from the insulating layer material. Using these deposition processes, a variety of materials, such as Pyrex and Haynes alloy, may be used for the substrate. The critical temperature and current values obtained for the two YBCO layers of the completed structure were on the order of 85 K and 2×10^5 A/cm^2, respectively. © *1996 American Institute of Physics.* [S0021-8979(96)06904-X]

I. INTRODUCTION

One of the potential applications of yttrium–barium–copper–oxide ($YBa_2Cu_3O_{7-x}$ or YBCO) films is as the electronic interconnects on a multichip module (MCM) substrate. By using the interconnected mesh power system (IMPS) MCM topology, a superconducting MCM can be realized with two levels of superconducting interconnection.[1] This is possible because the use of superconductor material for the interconnects allows for very high wiring densities. Thus, in order for this application to be realized, a large-area film of YBCO must be deposited onto a substrate, followed by a fairly thick layer of dielectric material, and finally, a second layer of YBCO. The thick layer of dielectric material is required to provide impedance control of the interconnect lines. As an additional constraint, the dielectric must have a relatively low dielectric constant in order to minimize the thickness of this layer.

Most efforts directed at the fabrication of multilayer YBCO structures have required each of the layers to maintain epitaxy of the substrate throughout the thickness of the structure.[2] This requirement greatly constrains the choice of substrate and dielectric materials that can be used. The materials must be chemically compatible with YBCO, and their lattice constants and coefficients of thermal expansion (CTE) must closely match that of YBCO.

Ion-beam assisted deposition (IBAD) is a technique which eliminates the constraint of maintaining epitaxy throughout the entire structure. This is due to a combination of the mechanisms of preferential sputtering, ion channeling, and shadowing of misoriented grains by the ion beam. The formation of a textured microstructure results from the higher sputtering yields of all orientations other than that of the channeling direction. Thus, a textured microstructure can be formed by carefully balancing the deposition rate with the sputtering due to the ion beam. Using IBAD, epitaxial films have been grown on top of amorphous layers. IBAD has been used to deposit textured yttria-stabilized zirconia (YSZ) on Pyrex[3,4] and Haynes alloy[4–7] substrates, and cerium dioxide has been used as a buffer material on these and other substrate materials.[8]

II. EXPERIMENT

In this article, YSZ was first deposited onto Pyrex substrates using IBAD under the deposition conditions outlined in Ref. 4. Briefly, the ion gun was positioned at a distance of 80 mm from the substrate and at an angle of 55° from the substrate normal. Argon gas was flowed through the gun at a rate of 20 sccm and an acceleration potential of 300 eV was used, with a beam current of 7 mA and a deposition pressure of 0.7 mTorr. The thickness of the YSZ layer was about 5000 Å. Next, YBCO was sputter-deposited to a thickness of 3000 Å using an off-axis configuration. The substrate was heated to 735 °C at a deposition pressure of 200 mTorr in an 80% argon/20% oxygen gas mixture. The YBCO was then capped with a 2000 Å thick layer of IBAD/YSZ to prevent interdiffusion. Next, a 4 μm thick layer of silicon dioxide (SiO_2) was deposited on top of the YSZ layer by reactive sputtering of a 3 in. diameter pure silicon target. The conditions were as

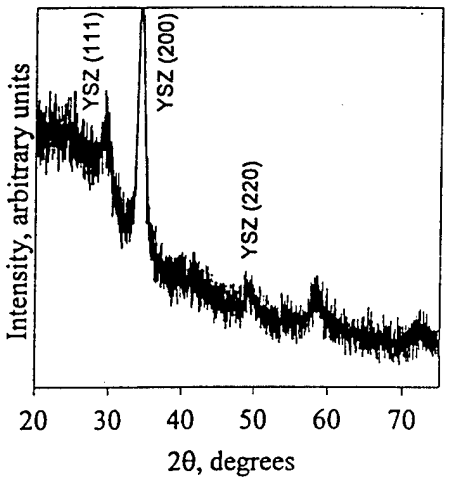

FIG. 1. Theta-two theta scan for a typical YSZ film deposited on Pyrex.

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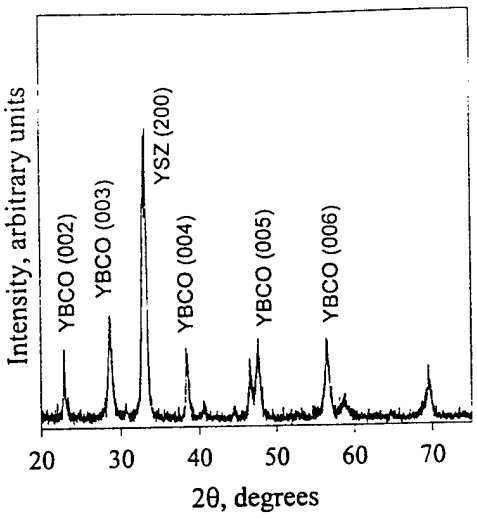

FIG. 2. Theta-two theta scan for a typical YBCO/YSZ structure deposited on Pyrex.

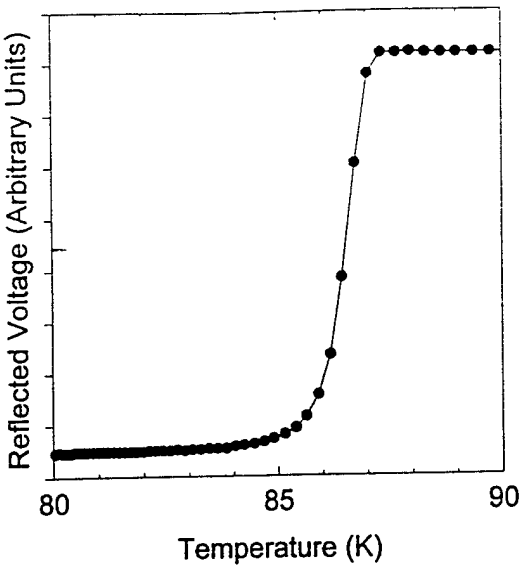

FIG. 3. The critical temperature curve of the YBCO shown in Fig. 2.

follows: a target-substrate distance of 50 mm, a pressure of 15 mTorr, an 80% Ar/20% O_2 gas mixture, and a rf power level of 200 W. The deposition rate was ~1 μm/h, and the films were deposited at room temperature (the substrate temperature generally increased to ~120 °C during deposition). The film thickness and index of refraction were measured by ellipsometry.

After the SiO_2 was deposited, a 5000 Å thick layer of YBCO/YSZ was deposited on the structure, and finally, 3000 Å of YBCO was deposited on top of the YSZ. All of the depositions were performed *in situ*; the YBCO depositions were performed with an off-axis geometry, and the SiO_2 and YSZ depositions were performed on-axis. During target change operations, the substrate was pulled into a load lock and pumped down to prevent reactions with the atmosphere.

III. RESULTS AND DISCUSSION

Figure 1 shows a theta-two theta scan for YSZ deposited on Pyrex. The (200) peak is clearly visible above the background which confirms orientation normal to the substrate surface. The phi scan of the YSZ (111) family of peaks for the same film reveals strong in-plane alignment. In Fig. 2, a theta-two theta scan for YBCO/YSZ deposited on Pyrex is presented. Only *c*-axis YBCO growth is visible in addition to the (200) YSZ. The phi scan of the YBCO (103) family of peaks (not shown in Fig. 2) reveals strong biaxial alignment, although grain boundaries are most likely present.

The critical temperature, T_c, curve of the YBCO film is shown in Fig. 3. This layer exhibited a T_c of 87 K and the critical current, J_c, measured using a noncontact method, was found to be 8×10^5 A/cm^2 at 77 K. Degradation of the superconducting properties of the bottom YBCO layer, due to subsequent film depositions, was determined by depositing all the remaining required layers except for the second layer of YBCO. To simulate the effects of the second YBCO deposition, the film stack was ramped to 735 °C and held at this temperature for 4 h. This approach to determining the degradation effects of subsequent depositions was necessary to prevent interference with T_c/J_c measurements on the bottom YBCO layer. Measurements of the superconductor properties of the bottom YBCO layer were then performed. The T_c and J_c degraded to 84 K and 2×10^5 A/cm^2, respectively. These data were confirmed separately by transport measurements. The reasons for these reductions is most likely due to oxygen effusion from the YBCO caused by the high temperature and long dwell time.[9]

The thick SiO_2 and subsequent layers were thoroughly inspected for cracks under an optical microscope, and none were found. The stress on all of the film layers is determined by the coefficient of thermal expansion (CTE) of the Pyrex substrate, which is higher than that of the films. The substrate is also several orders of magnitude thicker than the films. This is in agreement with Yin *et al.*[10] who found that films

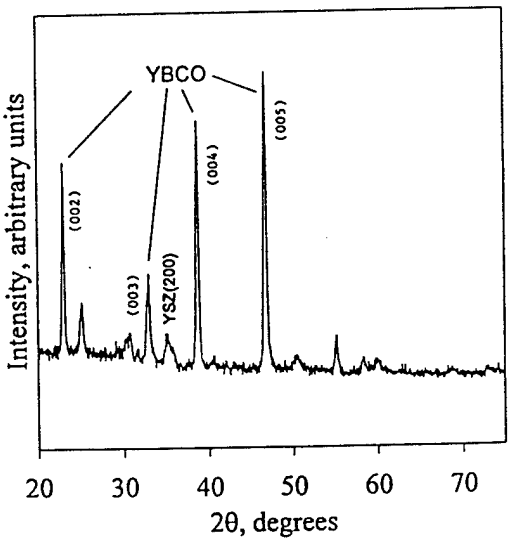

FIG. 4. Theta-two theta scan of the top YBCO layer.

with a smaller CTE than that of the substrate did not crack because they are under compressive stress.

A theta-two theta scan for the top YBCO layer of the structure is shown in Fig. 4. The T_c of the top layer of YBCO was determined using a contact measurement, and was found to be 86 K. It should be noted that the noncontact method cannot be used in this case due to interference by the bottom YBCO layer on the T_c measurements. To avoid patterning of the film, the J_c was measured with a noncontact method and was found to be 2×10^5 A/cm^2. This slightly lower value of J_c than was obtained for the bottom layer of YBCO can be attributed to the high-angle grain boundaries which are visible from the phi scan of the (103) YBCO peaks.

Among the factors that influenced the overall quality of the structure was film roughness. The roughness, as measured by atomic force microscopy, was observed to increase as the number of layers increased. The mean surface roughness of the top-most YSZ layer was measured to be 193 nm, which can easily disrupt the YBCO lattice.

IV. SUMMARY AND CONCLUSIONS

A multilayer structure consisting of two layers of superconducting YBCO separated by a relatively thick layer ($\approx$4 μm) of SiO_2, has been successfully fabricated using ion beam assisted magnetron sputtering. Buffer layers of ion beam assisted magnetron sputtered YSZ were used to separate the YBCO from the substrate material (Pyrex) and the SiO_2. The SiO_2 was deposited by reactive sputtering of a pure silicon target. The T_c and J_c of the bottom layer of YBCO was slightly degraded to 84 K and 2×10^5 A/cm^2, respectively, by the subsequent high temperature processing. The T_c and J_c of the top YBCO layer were similar to the final values of the bottom layer. These lower values for the top layer are attributed to increasing film roughness as the number of layers of material increases. However, the results of this article indicate that multiple levels of YBCO, required for the fabrication of a superconducting multichip module, can be successfully deposited on a variety of substrate materials using ion beam assisted magnetron sputtering of YBCO and YSZ buffer layers.

ACKNOWLEDGMENTS

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Magnetic field and temperature dependence of critical current densities in multilayer $YBa_2Cu_3O_{7-\delta}$ films

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In order to build high-temperature superconductor (HTS) multichip modules (MCMs), it is necessary to grow several epitaxial layers of YBCO that are separated by thick dielectric layers without seriously affecting the quality of the YBCO layers. In this work, we have successfully fabricated YBCO/YSZ/SiO_2/YSZ/YBCO structures on single-crystal $LaAlO_3$ substrates using a combination of pulsed laser deposition for the YBCO layers and ion-beam-assisted rf sputtering to obtain biaxially aligned YSZ intermediate layers. The bottom YBCO layer had a $T_c \sim 89$ K, $J_c \sim 7.2\times10^5$ A/cm^2 at 77 K, whereas the top YBCO layer had a $T_c \sim 86$ K, $J_c \sim 6\times10^5$ A/cm^2 at 77 K. The magnetic field and temperature dependence of J_c for the YBCO films in the multilayer have been obtained. The results for each of the YBCO layers within the YBCO/YSZ/SiO_2/YSZ/YBCO structure are quite similar to those for a good quality single-layer YBCO film. © *1996 American Institute of Physics.* [S0021-8979(96)03308-9]

I. INTRODUCTION

In electronic applications of high-temperature superconductor (HTS) thin films, the critical current density (J_c) is an important characteristic. One of the potential applications of high-temperature superconducting films is as electronic interconnects on a multichip module (MCM).[1] Since there are a minimum of two HTS thin films, separated by thick dielectric layers required, in HTS multichip modules (MCMs), it is necessary to know if the quality of the HTS layers is still maintained after the entire fabrication process is completed. In addition to the critical temperature (T_c) and critical current density at zero field, the dependence of J_c on an externally applied magnetic field and the temperature for the entire multilayer structure is crucial information for electronic applications. The YBCO/YSZ/SiO_2/YSZ/YBCO multilayer structure has been fabricated by Reade *et al.*[2] They reported cracking in the top YBCO layer, which limited their investigation of the properties of the multilayered structure.

In this article, we report a study of the temperature and magnetic field dependence of J_c for both YBCO layers in a YBCO/YSZ/SiO_2/YSZ/YBCO multilayer structure[3] performed by the magnetization method. Our results show that the temperature and magnetic field dependence of J_c of the YBCO layers of these samples are similar to those of high quality single-layer YBCO thin films.

II. EXPERIMENT

The YBCO/YSZ/SiO_2/YSZ/YBCO multilayer samples investigated here were prepared by using a combination of pulsed laser deposition and ion-beam-assisted magnetron sputtering. Details of the technique will be described elsewhere.[3] In short, a 200-nm-thick $YBa_2Cu_3O_{7-\delta}$ (bottom YBCO, layer 1) film was deposited on a single-crystal $LaAlO_3$ substrate (100 orientation and area 1×1 cm^2) by pulsed laser ablation at a substrate temperature of ~750 °C. Ion-beam-assisted rf sputtering was used to deposit biaxially aligned 200-nm-thick yttria-stabilized zirconia (YSZ) as a capping layer (layer 2). Next a 1-μm-thick, amorphous SiO_2 layer (layer 3) was deposited on layer 2 at room temperature by rf sputtering. The capping layer (YSZ) is used to prevent diffusion of the third SiO_2 layer into the top YBCO layer. A fourth layer (biaxially aligned YSZ) was then deposited on the SiO_2 layer to a thickness of 200 nm using the same method as for layer 2. This layer is very important. It not only functions as protection against the diffusion of the third SiO_2 layer into the YBCO layer, it also allows good epitaxial YBCO growth if it has a well-aligned structure. Finally, the top YBCO layer (layer 5) was deposited by laser ablation under the same conditions as was used for layer 1.

The orientation of the YSZ and YBCO layers was characterized by x-ray diffraction. The magnetization $M(H)$ loop was measured using a Quantum Design Magnetometer in fields up to 4 T, applied parallel to the c-axis direction and at a fixed temperature. This was repeated for different temperatures ranging from 5 to 77 K. The values of J_c were calculated using Bean's model. The electrical resistance was measured using the standard four-lead technique.

III. RESULTS AND DISCUSSION

X-ray diffraction data showed that all samples investigated here were single-phase highly c-axis oriented with very good in-plane epitaxy (Fig. 1). There were no cracks observed in the top YBCO layer. The resistance $R(T)$ and magnetization $M(T)$ of the samples were carefully measured for each YBCO layer. Figure 2 shows the typical resistance as a function of temperature for the top YBCO layer. The

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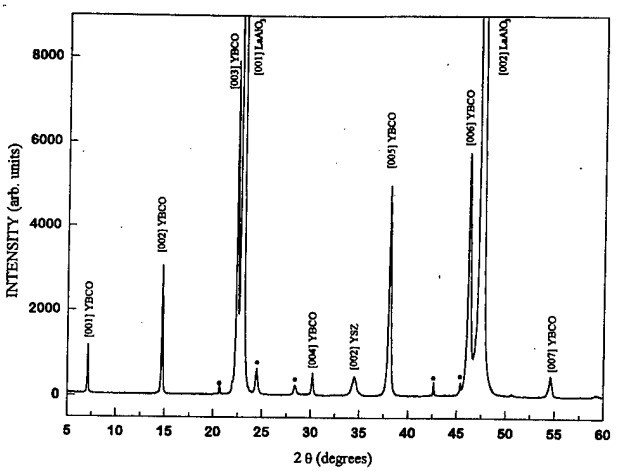

FIG. 1. θ-2θ x-ray diffractometer pattern for the YBCO/YSZ/SiO_2/ YSZ/ YBCO structure on [001] $LaAlO_3$ (*: indicate substrate impurity peaks seen in the bare substrates of the same batch).

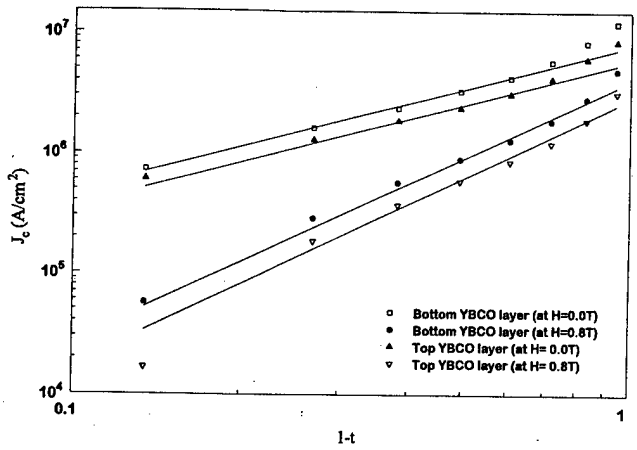

FIG. 3. Logarithmic plots of J_c vs $1-t$ for each of the YBCO layers within the multilayer structure. Straight lines are the curve fits to $(1-t)^n$, where $n\sim1.3$ for $H=0.0$ T and $n\sim2.1$ for $H=0.8$ T.

zero resistance temperature for this YBCO layer is about 86 K with a transition width of about 2 K. The $M(T)$ data for a multilayer sample are shown in the inset of Fig. 2. As can be seen in the inset of Fig. 2, the onset transition of the $M(T)$ curve is about 89 K. A second transition (indicated by the arrow in the inset of Fig. 2) is consistent with the T_c of the top YBCO layer measured by the transport method (Fig. 2). In order to verify this, T_c was remeasured again after the top layer of YBCO was etched away by using a dilute EDTA solution, and the onset transition was found to be about 89 K.

The critical current density J_c of the samples were measured by the magnetization method and calculated using Bean's model. For a rectangular single-layer film, J_c can be calculated from the following formula:[4]

$$J_c = 10[M_+(H) - M_-(H)]/L_1[1-(L_1/3L_2)]V. \quad (1)$$

In Eq. (1), $M_+(H)$ and $M_-(H)$ are the magnetization of the decreasing and increasing field branches in electromagnetic units (emu), respectively; V is the volume of the thin film in cm^3; L_1 and L_2 are the short and long sides of the samples in cm, respectively. We have assumed that J_c is independent of the B field and excluded the anisotropic critical currents in the above calculation. In order to determine J_c of both the top and bottom YBCO layers, the magnetization $M^m_+(H)$ and $M^m_-(H)$ for the multilayer film was measured first, then the magnetization $M^b_+(H)$ and $M^b_-(H)$ for the bottom layer was measured after the top layer of YBCO was etched away. In this article we use superscript t and b for the parameters related to the top and bottom YBCO layer in the multilayer film, then J_c for the bottom layer should be

$$J^b_c = 10[M^b_+(H) - M^b_-(H)]/L^b_1[1-(L^b_1/3L^b_2)]V^b, \quad (2)$$

and for the top layer in the multilayer film,

$$J^t_c = 10\{[M^m_+(H) - M^b_+(H)] - [M^m_-(H) - M^b_-(H)]\}/L^t_1[1-(L^t_1/3L^t_2)]V^t. \quad (3)$$

The J_c of the top YBCO layer was found to be about 6×10^5 A/cm^2, and a value of $\sim7.2\times10^5$ A/cm^2 was obtained for the bottom layer at 77 K under zero magnetic field. J_c, as a

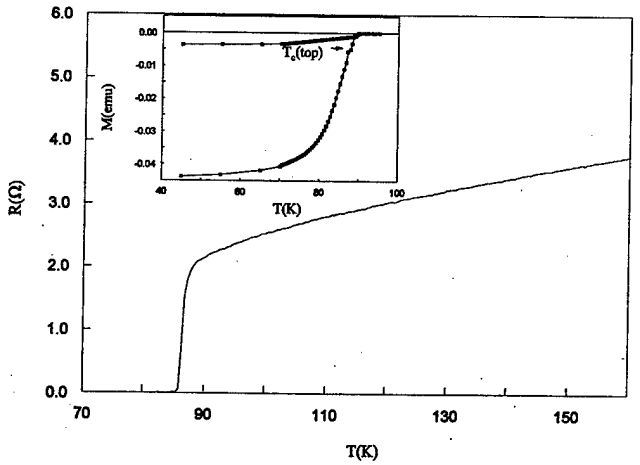

FIG. 2. Resistance vs temperature for the top YBCO layer in the YBCO/ YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ multilayer structure. Inset: magnetization M as a function of T for the entire multilayer structure.

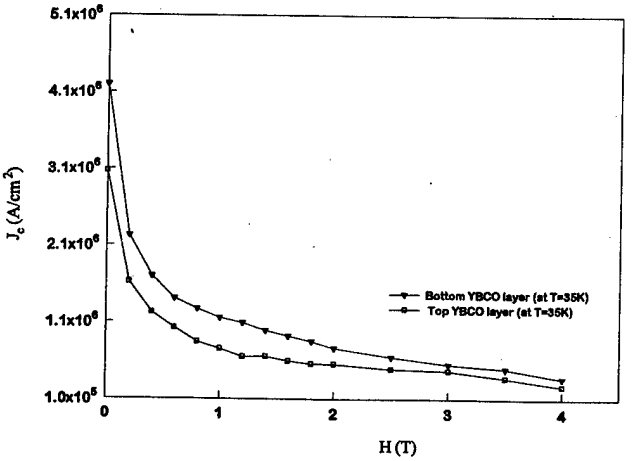

FIG. 4. Magnetic field dependence of J_c for top and bottom YBCO layers at 35 K. Field is applied perpendicular to $a-b$ plane.

function of $(1-t)$, is shown in Fig. 3 for different values of the magnetic field, where $t=T/T_c$. It was found that, for both YBCO layers, the temperature dependence of J_c is similar to that for a good quality, single-layer YBCO film.[5–7] The magnetic field dependence of J_c for both YBCO layers at 35 K are shown in Fig. 4. It clearly shows that J_c for both top and bottom YBCO films essentially has the same magnetic field dependence as that for the high quality, single-layer YBCO film.[5–7]

IV. SUMMARY

A good quality YBCO multilayer structure has been fabricated using laser ablation and ion-beam-assisted rf sputtering. The dependence of J_c on the temperature and magnetic field for both YBCO layers in the multilayer has been determined. The results suggest that the temperature and magnetic field dependence of J_c of the YBCO layers in the multilayer structure are not altered appreciably by the multilayer growth processes.

ACKNOWLEDGMENTS

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FABRICATION OF HIGHLY TEXTURED SUPERCONDUCTING THIN FILMS ON POLYCRYSTALLINE SUBSTRATES USING ION BEAM ASSISTED DEPOSITION

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ABSTRACT

$Tl_2Ba_2CaCu_2O_y$(Tl2212) thin films on ceramic Al_2O_3 substrates with J_c(77K) of about 10^5 A/cm^2 and high quality YBCO/YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ mutilayers with J_c(77K) of about 6×10^5 A/cm^2 in the top YBCO layer have been successful deposited for the first time. These Mirror-like, highly c-axis oriented films were grown on highly textured YSZ buffer layers, which were deposited through Ion Beam-Assisted Laser Ablation. The zero resistance temperature is 95-108K for the Tl2212 films, and 85-90K for the multilayer YBCO films. The results suggest that using cheap non-single crystal substrates to fabricate good HTS films is possible.

I. Introduction

Since the discovery of high temperature superconductors(HTS), many possible applications of HTS thin films have been design and demonstrated, from very useful fault current limiters to the electronic interconnects on multichip module (MCM) substrates. All of these applications would benefit from the use of HTS thin films. One of the major problems for the application of HTS's is that HTS's can carry only a limited amount of current without resistance. This problem is related to their two dimensional layered structure. According to earlier studies[1-2], if the layers do not line up properly, the critical current density will decrease dramatically in the misaligned region. One way to overcome this problem is to grow micron-thin layers of the material on well organized substrates, epitaxally. The process has the effect of lining up the superconducting layers more accurately. HTS thin films grown on single crystal substrates of $LaAlO_3$ or $SrTiO_3$ have good lattice match between the HTS and substrate, and have critical current densities of about ~10^6 A/cm^2, which is large enough for most HTS thin film applications. While this effort is impressive, it is far from useful, since the films so developed are much too expensive because the single crystal substrates are very expensive and available only in relatively small sizes. Moreover, for some electronic applications such as HTS multi-chip modules(MCM's),

there are at least two HTS thin films that are separated by thick dielectric layers. Useful dielectric layers such as SiO_2 have noncrystalline structures. For this reason, HTS thin film layers cannot be grown on the dielectric layer with good alignment by conventional methods. Recent studies[3-7] have shown that highly biaxially aligned YSZ layers can be grown on non-crystalline substrates, which are cheaper and easy to get in any size needed by Ion beam-assisted laser deposition(IBAD). Using this method, high quality $YBa_2Cu_3O_y$ (YBCO) films have been deposited on biaxially aligned YSZ layers grown on non-crystalline substrates with J_c's of up to 8×10^5A/cm^2 at 75K.

Here, we report the results from Tl2212 films fabricated on polycrystalline Al_2O_3 substrates with an IBAD deposited YSZ buffer layer and YBCO/YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ mutilayers.

II Experimental

Fine polished Al_2O_3 was used for the substrates of the Tl2212 films. Ion-beam assisted pulsed laser deposition was used to prepare highly biaxial aligned YSZ buffer layers at room temperature. While YSZ was deposited by pulse laser deposition, an Ion-beam (argon ion source) bombarded the substrates at an angle of 55° from the substrate normal. The laser used here was an ArF excimer laser (wavelength = 193 nm, shot frequency = 5 Hz). The energy density of the laser beam, which was focused on the YSZ target, was set to about 2 - 3 J/cm^2. The ion beam energy was typically set at about 250 eV, and the beam current density was about 120 μA/cm^2. The oxygen partial pressure was maintained at 3×10^{-4} Torr, and with the ion beam the total pressure in the vacuum chamber was about 8×10^{-4} Torr during the deposition of the YSZ layers. The substrate temperature increased to about 100 °C due to the assisting ion beam. The growth rate was about 0.5 Å/S. The thickness of the YSZ buffer layers in our experiment was about 5000 Å. For the YBCO multilayer structure, 2000 Å thick YBCO layers were deposited by pulsed laser ablation at ~ 750 °C. A 4-5 micron thick amorphous SiO_2 layer was deposited as a dielectric layer at room temperature by rf sputtering. For the Tl2212 films, 2000~3000Å $Ba_2CaCu_2O_y$ precursor films were deposited on the YSZ-buffer layer at a temperature of 400°C using pulsed laser ablation. The films were then treated in a thallination process at 810°C.

The structures of deposited films were characterized by x-ray diffraction. T_c and J_c of HTS layers were measured by both transport method using the standard four-lead technique and the magnetization method using a Quantum Design Magnetometer.

III. Results and Discussion

All YSZ films deposited on the polycrystalline Al_2O_3 substrates for Tl2212 or on first YBCO layer, or on amorphous SiO_2 layer were (001) oriented with the <001> axis normal to the substrate plane. A typical X-ray θ-2θ diffraction pattern for a YSZ film deposited on a polycrystalline Al_2O_3 substrate is shown in Fig.1. Observation of only the YSZ(002) peak in the

X-ray θ-2θ diffraction pattern indicates that the YSZ was highly (001) oriented. The ϕ scan width of the {111} peaks is about 25° (FWHM).

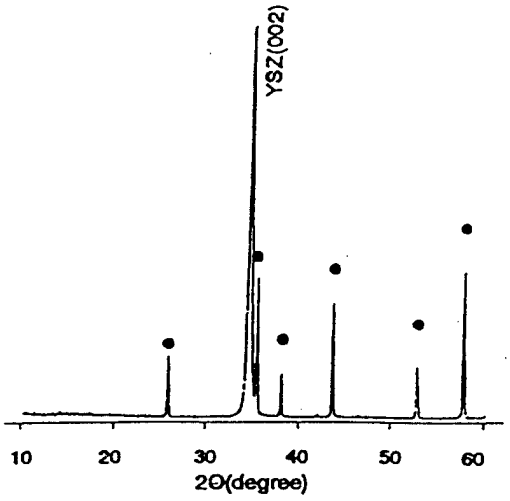

Fig. 1. X-ray diffraction θ-2θ scan of YSZ on Al_2O_3 (● Al_2O_3 peak)

Typical resistance versus temperature data for Tl2212 is shown in Fig.2. The zero resistance temperature T_c is 105.6K which is comparable with the results from the high quality films grown on $LaAlO_3$ or $SrTiO_3$ substrates. The critical current densities of these films are about 8×10^4 A/cm^2 by transport method. Fig.3 shows the typical resistance as a function of temperature for the top YBCO layer in the multilayer structures. The zero resistance temperature for this YBCO layer is about 86K with a transition width of about 2 K. The Messier effect M(T) for the same mutilayer sample is shown in the inset of Fig.3. As in the inset of Fig.3, the onset transition of the M(T) curve is at about 89 K, a second transition (indicated by the arrow) in the inset of Fig.3 is consistent with the T_c of the top YBCO layer measured by the transport method (Fig.3). In order to verify this, T_c was remeasured again after the top layer of YBCO was etched

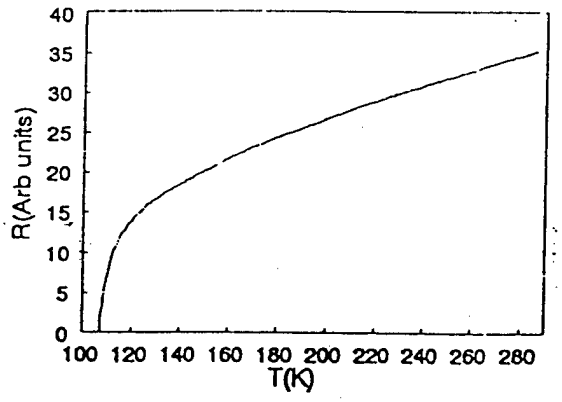

Fig. 2. Resistance vs. Temperature for the $Tl_2Ba_2CaCu_2O_8$ on YSZ/Al_2O_3.

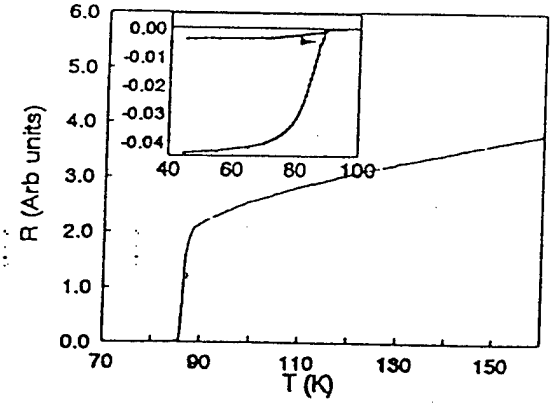

Fig. 3. Resistance vs temperature for the top YBCO layer in the YBCO/YSZ/SiO_2/YSZ/YBCO/ $LaAlO_3$ multilayer. Inset: Magnetization M as a function of temperature for the entire multilayer.

away by using a dilute EDTA solution, and the onset transition was found to be at about 89 K without the second transition. The critical current density, J_c of the samples were measured by the

magnetization method and calculated using Bean's model before and after the top layer of YBCO was etched away. The J_c of the bottom YBCO layer is about 7.2×10^5 A/cm^2 at 77 K, and of the top YBCO layer is about 6×10^5 A/cm^2 at 77 K, For comparison, we deposited both YBCO and Tl2212 on ceramic Al_2O_3 substrates. Even though the T_c of these films were about the same, J_c is $< 10^4$ A/cm^2. Which is about two orders of magnitude lower than that of the film on the biaxially aligned YSZ layer

IV. SUMMARY

Tl2212 films on ceramic Al_2O_3 substrates have been grown for the first time and good quality YBCO multilayer structures have been prepared using laser ablation and ion beam assisted rf sputtering. Our results demonstrate that good quality HTS films can be grown on cheap nonsingle crystal substrates though the Ion Beam-assisted deposition technique.

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Recent Advances in High Temperature Superconductor Multichip Modules

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Abstract

Two different techniques for fabricating high temperature superconducting (HTS) MCM-D substrates have been developed and tested. The first unit consists of two digital gallium arsenide bare die connected by $YBa_2Cu_3O_{7-\delta}$ (YBCO) HTS interconnects to form two ring oscillators on a 2.25 cm² MCM-D substrate. The interconnections consist of two wiring layers of YBCO separated by a 4-5 μm silicon dioxide interlevel dielectric. The signal lines are routed between power and ground lines which form an interconnected mesh power system (IMPS) and, thereby, the module avoids the necessity of having two additional layers for power and ground planes. Connection between the two YBCO layers is accomplished with low contact resistance 40 μm gold vias through the interlevel dielectric layer. The signal interconnects have 50 μm linewidths and 75 μm spacings. Electrical connections between the die and the MCM substrate and between the substrate and the PC board were made using ultrasonic Al wire bonds to low contact resistance gold/YBCO bond pads on the MCM substrate.

The second module, known as the Flip-Mesh superconducting MCM, provides an alternative to the multilayer MCM-D substrate described above. It involves using flip chip bonding techniques to connect multiple single-layer substrates, thereby reducing the processing complexity of fabricating multiple layers. X-plane and Y-plane interconnects are fabricated on separate substrates and interconnected using solder bumps. The IMPS topology is also utilized in this structure so that power, ground, and signals can be fabricated on two planes. The initial Flip-Mesh design incorporates 100 μm (4 mil) solder bump vias with similar spacings, which results in a low packing density for MCM-D technology, but a high density for I/O technology.

Key words: High temperature superconductors, MCM-D, Interconnected Mesh Power System (IMPS), YBCO

Introduction

Unlike that of VLSI technologies where smaller feature sizes in successive generations allow interconnect lengths and power dissipation to be reduced, multichip modules (MCMs) will not have that same luxury. As the complexity of ICs advances, pinout count per IC increases, and operating frequencies increase, MCM normal metal interconnections will have to grow in length and will not be allowed to reduce in cross-sectional area. On MCM-D substrates, typical copper or aluminum interconnection dimensions are about 2 to 5 μm in thickness and between 15 and 30 μm wide. The resistivity of copper or aluminum decreases by at least a factor of 7 when decreasing the temperature from 300 K to 77 K (liquid nitrogen temperature), which allows smaller cross-section interconnections to be fabricated on cryo-cooled MCMs. In order to increase the wiring density in MCMs beyond that of cryo-cooled MCMs and improve the chip-to-chip bottleneck at high frequencies, alternatives to conventional metal interconnects must be considered [1].

High temperature superconductor (HTS) interconnections, with negligible resistivity at operating frequencies of several tens of GHz and lower, have great potential to reduce the interconnection line cross-section even further with typical thicknesses being less than 1 μm and widths could be reduced to less than 2 μm for MCM applications. The critical current density of HTS interconnects, which limits the line's minimum cross-section, is similar in value to the maximum current density allowed in Al interconnects to inhibit electromigration. These small, low resistance

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interconnects offer significant performance advantages over normal metal interconnects for MCM-D technology using CMOS or GaAs integrated circuits which have enhanced chip level performance at liquid nitrogen temperatures (77 K). An added benefit of HTS lines is the reduced capacitive coupling between adjacent interconnections (due to their reduced thickness) which allows the lines to be spaced more closely together. The reduced cross-section of HTS interconnects should allow a significant increase in packing density and a corresponding decrease in the number of interconnect layers required to achieve the same functionality with normal metal interconnects.

We have been developing two separate HTS MCM prototypes. One is to be the first planar HTS MCM utilizing a thick layer of silicon dioxide as an interlevel dielectric and is based on MCM-D technology. The second prototype is based on interconnecting two layers of HTS interconnects on separate substrates via solder bumps and flip chip techniques. Our development has centered around the HTS material $YBa_2Cu_3O_{7-\delta}$ (YBCO) which has a transition temperature of about 91 K (well above the boiling point of liquid nitrogen, 77 K) and critical current densities typically greater than 5 x 10^5 A/cm^2.

I. HTS MCM-D Prototype

A cross-section of our proposed HTS MCM is shown in Figure 1.

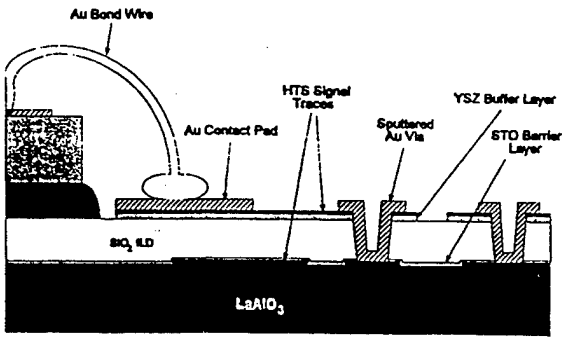

Figure 1. HTS MCM cross-section.

This novel structure has several key features that provide advantages over previously demonstrated HTS MCMs [2,3]. These advantages are:

(1) the utilization of an Interconnected Mesh Power System (IMPS) topology that is ideal for HTS multilayer fabrication because it allows an MCM to be constructed with only two layers of interconnects as opposed to the four that are traditionally used: x-signal, y-signal, and ground and power planes;

(2) a thick (~ 5 μm) layer of SiO_2 that is sandwiched between a thin buffer layer dielectric and a thin diffusion barrier layer dielectric to form a composite interlevel dielectric that is compatible with multilayer YBCO processing while allowing controlled impedance (Z_o = 50 Ω) lines to be fabricated, which are necessary for high speed signal propagation;

(3) chemical-mechanical polishing to create a planar SiO_2 surface for deposition of a high quality top level superconductor/buffer layer;

(4) high-aspect ratio, low contact resistance vias that utilize noble metals to form contacts between the two layers of YBCO interconnects, as opposed to large area, low-aspect ratio superconducting vias that have been fabricated with marginal success previously.

Due to the grain boundary problems associated with making very wide, sloping superconducting vias through a thick dielectric layer, alternative methods have to be explored to create the compact, high-aspect ratio vias necessary for fast, high density HTS MCMs.

Yttria stabilized zirconia (YSZ) was chosen as the material for providing a diffusion barrier/buffer layer between the superconductor and the interlevel dielectric material, silicon dioxide, because of its diffusion barrier properties as well as having a close lattice spacing and coefficient of thermal expansion (CTE) match to YBCO. Silicon dioxide was chosen as the interlevel dielectric material because of its low dielectric constant and well developed deposition and etching processes.

Experimental Details

Our MCM-D substrate was constructed of two layers of laser-ablated YBCO interconnects separated by a multilayer dielectric consisting of $SrTiO_3/SiO_2/YSZ$. We are able to attain critical current densities > 5 x 10^5 A/cm^2 in both YBCO layers. The laser-ablated $SrTiO_3$ (STO) and ion beam assisted laser-ablation deposited (IBAD) YSZ (yttria-stabilized zirconia) layers were ~0.5 μm thick while the reactively-sputtered SiO_2 ranges between 4 and 5 μm thick. The multilayered thin film structure is fabricated on 15 mm x 15 mm $LaAlO_3$ and YSZ substrates.

The HTS MCM was layed out as shown in Figure 2 on the following page.

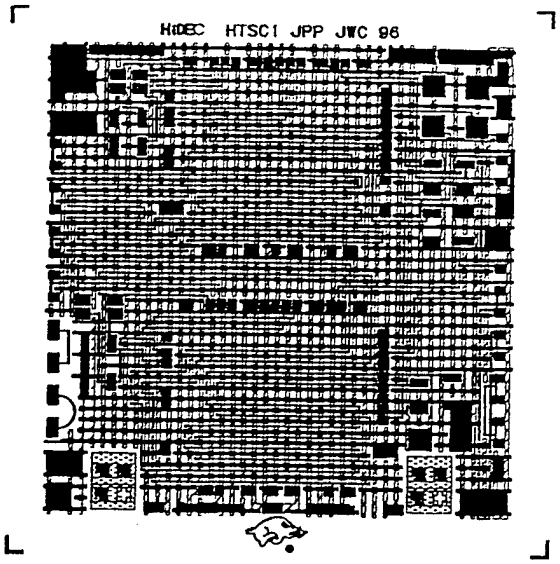

Figure 2. Layout of a 2 layer 15 mm x 15 mm HTS MCM-D substrate.

The 2.25 cm^2 substrate consists of two separate ring oscillators built using YBCO interconnects between two digital GaAs bare die (4.4 mm x 3.5 mm). The first ring oscillator is connected using the smallest possible interconnection, whereas, the second is connected by a much longer interconnect. A performance comparison between the two oscillators is planned for future work. There are also bond pads on the substrate for mounting various sizes of surface mount decoupling capacitors and terminating resistors. A prototype of our ring oscillator using one of the GaAs bare die wirebonded to 20 mil wide copper traces on a PC board was tested at liquid nitrogen temperature and was found to oscillate at ~250 MHz. Based on this result, our HTS MCM ring oscillator is estimated to operate at about the same frequency.

The via fabrication process is shown in Figure 3. The etching involves a 500 eV ion mill through the top YSZ buffer layer, which is followed by a reactive ion etch (RIE) through the SiO_2 interlevel dielectric selectively stopping at the barrier layer of STO. To complete the etching process, a 500 eV ion mill is done to etch through the STO and into the underlying YBCO. The final milling is very nonselective and requires close observation to keep from overetching through the bottom layer of YBCO. When depositing the top layer of YBCO at ~700° C, whatever material is deposited on the via sidewalls is presumably corroded due to interdiffusion of Si from SiO_2 into the YBCO but, presumably, does not affect the quality of the via. The subsequent *in situ* deposition of ~2000 Å of Au by laser ablation creates low resistance contacts without having to do a high temperature anneal in oxygen as was described by Ekin et al. [4]. This Au capping layer also acts as a passivation layer for the YBCO. In similar structures, contact resistivities of less than 10^{-7} Ω-cm^2 have consistently been attained. An additional 1.5-2.0 μm of Au is deposited over the existing YBCO/Au and then patterned using ion milling and photoresist as a mask.

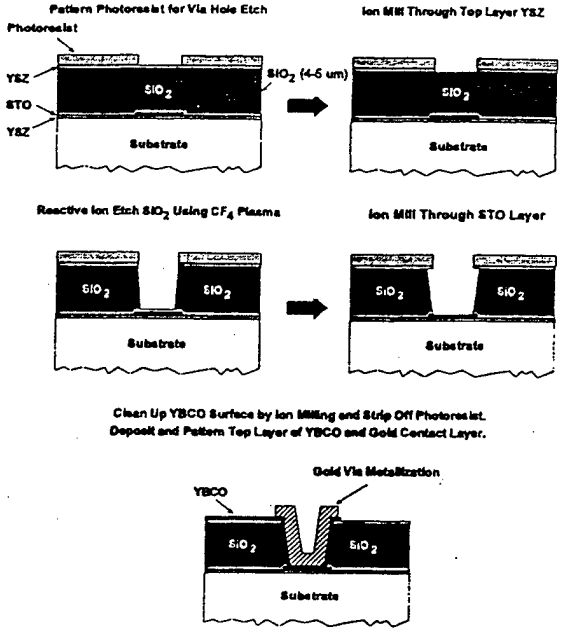

Figure 3. HTS via fabrication process.

This type of via structure has several advantages over previously demonstrated superconducting vias for use in HTS MCMs [2,3]. Since HTS thin films have to be deposited on planar surfaces or gradual slopes to maintain a reasonable current density, due to grain boundary problems, they require gradually sloped via holes that take up a wide area. By using a noble metal, compact, high-aspect ratio vias can be fabricated reliably.

Ultrasonic Al wire bonds were then made between YBCO/Au bond pads on the substrate and a wire bondable PC board. Via chain resistance was measured using a conventional 4-point contact configuration and measuring the voltage drop across the vias while passing DC current through it. The resistance vs. temperature of a ~0.5 cm long via chain structure with ten 40 μm square vias interconnecting 50 μm wide YBCO lines is shown in Figure 4. The room temperature resistance was measured to be about 515 Ω, and upon cooling to 78.5 K, the resistance dropped to about 87 Ω. As is shown in this figure, there are two separate superconducting transitions occurring at about 89 K and 80 K, which correspond to the top and bottom layer YBCO transitions. At 78.5 K, the interconnects had not yet become fully superconducting.

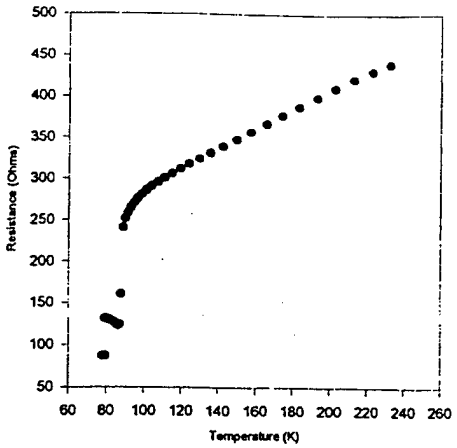

Figure 4. Temperature transition of a chain of ten 40 μm wide vias.

II. Flip-Mesh HTS MCM

The Flip-Mesh Superconducting Multi Chip Module (MCM) is an alternative to the conventional multi-layer superconducting MCM. It is desired that a superconducting MCM be fabricated using High-Temperature Superconductor (HTS) materials, with which such an MCM can be cooled using liquid nitrogen. However, many difficulties arise in the formation of multiple superconducting planes separated by dielectric layers on a single substrate. The crystalline nature of HTS materials such as Yttrium-Barium-Copper-Oxide (YBCO) requires that the deposition surface be closely matched to the HTS material in crystalline structure.

The high temperatures needed to form HTS materials requires that the other HTS MCM materials be matched with the superconductor in coefficient of thermal expansion (CTE), and not crack or delaminate at such high temperatures. These requirements lead to a complex stack of materials in order to create a multiple-superconducting-plane MCM interconnect structure. This combination of materials also complicates selective patterning processes with respect to the HTS material.

Flip-Mesh Basics

The fundamental concept of Flip-Mesh is that instead of depositing multiple HTS layers on a single substrate and connecting the layers by vias, single HTS layers are deposited on multiple substrates, and opposing superconducting layers on separate substrates are connected by flip-chip technology. This reduces the number of high-temperature processing steps to one, eliminating most of the difficulties in the multi-layer structure. However, the use of I/O technology to form vias limits the ultimate density of the Flip-Mesh Superconducting MCM.

In the multilayer MCM, Ion Beam Assisted Deposition (IBAD) [5] is used to form an oriented buffer layer so that an HTS film can be grown on an amorphous surface. This also allows the use of an amorphous substrate. Since Flip-Mesh requires only one superconducting plane per substrate, it is an ideal application for depositing HTS films on amorphous substrates. Amorphous substrates are considerably less costly than single-crystal substrates.

Flip-Mesh Substrate Arrangement

There are three substrates in a Flip-Mesh module. The main substrate contains *x*-plane interconnect and bonding sites for chips. Two smaller secondary substrates contain *y*-plane interconnect, and are "flipped" onto the main substrate. The chip bonding sites are between the secondary substrates. I/O pads are located on the outside edges of the main substrate. The Flip-Mesh substrate configuration is shown in Figure 5. As with the multilayer MCM, the Interconnected Mesh Power System (IMPS) topology [6] allows complete power, ground, and signals to be formed in two conducting planes. The term "Flip-Mesh" is derived from the flipping of IMPS-mesh interconnect planes to form an MCM interconnect structure.

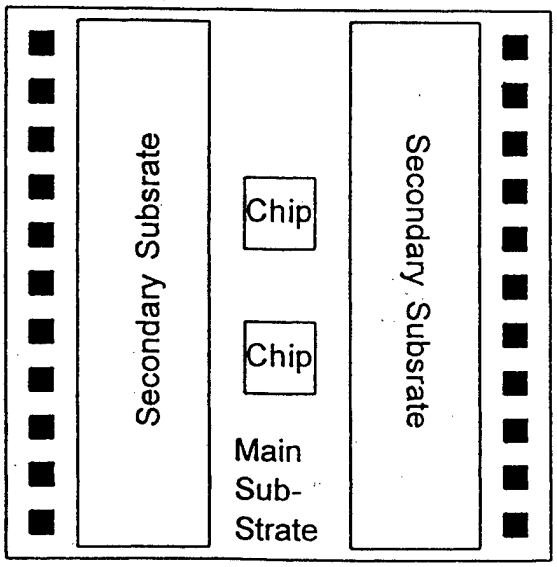

Figure 5. Flip-Mesh substrate configuration.

Flip-Mesh Substrate Processing

YBCO films are formed by laser ablation [7] on 1/2" or 1" square single-crystal yttria-stabilized zirconia (YSZ) or IBAD YSZ-buffered alumina substrates. The YBCO films are then patterned by argon ion milling [8] using conventional photoresist as a mask. The fact that ion milling is non-selective is not important in Flip-Mesh, since the underlying layer is always the substrate, which can be over-etched. The ion milling system is equipped with a water cooled sample stage to prevent YBCO or photoresist damage due to excessive heating from the ion milling.

Gold pads are then formed where electrical contact to YBCO is desired. A lift-off process is employed in which 2 μm of gold is sputter deposited onto a patterned photoresist layer. The Flip-Mesh substrates are exposed to a brief low-energy ion milling, which serves to prime the exposed YBCO surface for the gold deposition. After deposition, the photoresist layer is lifted off in an ultrasonic bath of acetone, leaving the gold pads on the YBCO. The lift-off process again avoids selective etching with respect to the YBCO. The Flip-Mesh substrates are then annealed at 600 °C for 1 hour in 500 Torr of oxygen to form a sturdy low-resistance contact.

The critical element of Flip-Mesh is the material used for the vias and the method used to form the interconnection. Figure 6 shows a cross-section of a Flip-Mesh via bump.

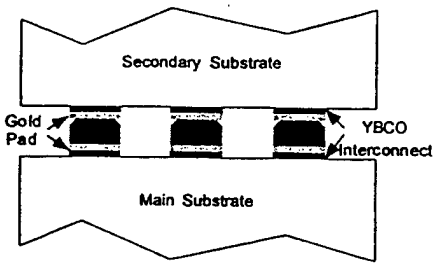

Figure 6. Flip-Mesh via cross-section.

The initial approach was to form gold balls using a ball bonding machine, and then press the substrates together while heating. Ball placement was found to be tedious, but workable. It was discovered, however, that the ball bonding process would often damage the underlying YBCO. This was not obvious unless the gold ball detached from the bonding pad. Ball detachment can be avoided by attaching to a bonding pad that is at least 1.5 times the size of the ball, but it is believed that this only disguises the damage.

Typical gold ball sizes range from 70 μm to 100 μm in diameter. The size of the Flip-Mesh bonding pad is 100 μm. Since density is already a limiting factor in the Flip-Mesh approach, increasing the via size is not desirable. It was also found that the extreme heat and pressure required to make an acceptable contact between the Flip-Mesh substrates caused the YBCO to become non-superconducting. The YBCO could be repaired by annealing, but the substrates would detach in the process.

The second assembly method attempted was to individually place preformed indium spheres. Indium was chosen because of its decent conductivity and low melting point. It was quickly discovered, however, that indium is far too soft to be handled mechanically, and no modules could be formed using this method. Stencil printing was then determined to be the ideal method for placing Flip-Mesh via bumps. A batch process would certainly be desirable, but the small via size (4 mil) and pitch (8 mil) puts severe limitations on this technology.

The first material to be screen printed was conductive epoxy, but this material was unable to meet the density requirement. The epoxy bumps would flatten and create shorts. Further work with the viscosity of the epoxy may lead to a useful application.

The next stencil printing material used was tin/lead solder. A special high-density solder was acquired, and worked nicely, but standard tin/lead solder has a leaching problem with the gold contact pads. Modules fabricated in this process detached within hours due to the leaching. Another solder paste was then acquired, which contained an additional 2% silver to prevent gold leaching.

After screen printing solder pads to the main substrate, the secondary substrates are aligned to the main substrate, and the solder is reflowed. The current Flip-Mesh material components are laser-ablated YBCO on single-crystal YSZ substrates with gold contact pads interconnected by screen printed tin/lead/silver solder bumps.

Initial Flip-Mesh Circuit

The initial Flip-Mesh circuit is a ring oscillator formed from 2 quad-XOR HCMOS chips. The first XOR gate has one input tied high, which turns it into an inverter. The other gates have one input tied low, which makes them buffers. This arrangement permits the number of gates in the loop to be adjusted from 2 to 8, allowing different speeds of oscillation.

The IMPS power and ground stripes are 250 μm wide, the signals are 50 μm wide, and the spacing between the two is 50 μm. The main substrate is 10

mm x 10 mm, and the secondary substrates are 2.5 mm x 10 mm. As was discussed previously, the contact pads are 100 μm x 100 μm. The XOR chips are approximately 1mm x 1mm each.

Flip-Mesh Assembly and Testing

After a Flip-Mesh substrate module is completed, the XOR chips are attached using thermoplastic tape. The leads of the chips are then aluminum wire bonded to the main substrate. The number of gates in the oscillator loop is selected by a wire bond in the center of the main substrate. The assembled Flip-Mesh module is then attached to a test board using thermoplastic tape. The I/O pads of the module are then aluminum wire bonded to the test board.

When complete, the test board is attached to an oscilloscope and power supply, measuring the output signal of the first XOR gate. The module is then slowly immersed in a small dewar of liquid nitrogen.

Conclusions

In summary, 40 μm YBCO/Au via chain structures have been characterized for use in an MCM-D substrate. The preliminary work shown here is to be improved upon by improving the quality of the YBCO layers, lowering the contact resistances, and possibly improving the step coverage of Au through the via by increasing its thickness. We are hoping to have an HTS MCM-D substrate fabricated in the near future. The performance of this MCM will be compared to that of a nearly identical Al interconnect module operating at liquid nitrogen temperature.

Thus far, functional Flip-Mesh modules have been fabricated only with metal interconnects. These modules were built on glass substrates with gold/titanium-tungsten metallization, and the substrates were interconnected with gold balls formed by a ball bonder. These units were tested both at room temperature and while immersed in liquid nitrogen with 2 to 8 gates in the oscillator loop. As would be expected, the modules ran faster at cryogenic temperature. While the gold ball vias worked adequately for a metal module, they were found to be incompatible with YBCO due to damage caused by the attachment process. The stencil printing processes discussed are under investigation to find a YBCO-compatible process. It will be interesting to compare the performance of the HTS Flip-Mesh to the cryogenic metal Flip-Mesh.

Despite the great processing complexity involved with fabricating an HTS MCM, great progress is being made toward achieving practical MCM substrates utilizing these novel materials.

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Physica C 282–287 (1997) 683–684

PHYSICA C

Fabrication and characterization of vias for contacting $YBa_2Cu_3O_{7-x}$ multilayers

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In order to connect multiple layers of high temperature superconductor (HTS) interconnects, low contact resistance vias must be used to maintain high signal propagation speeds and to minimize signal losses. In this work, 40 μm via contacts through $YBa_2Cu_3O_{7-x}$ /$SrTiO_3$/SiO_2/YSZ/$YBa_2Cu_3O_{7-x}$ multilayers utilizing dry etching techniques and sputter deposited Au for contacting through the vias have been successfully fabricated and characterized. The vias connect two laser ablated $YBa_2Cu_3O_{7-x}$ (YBCO) signal lines through thick (4-5 μm) SiO_2 insulating layers. This approach to making multilayer superconductor vias provides a low resistance contact between the YBCO layers while maintaining space efficiency and fabrication compatibility with the superconductor.

1. INTRODUCTION

Since the discovery of high temperature superconductivity (HTS), researchers have utilized their low resistance behavior in many applications. One such application is that of multichip modules (MCMs.) Unlike that of VLSI technologies where smaller feature sizes in successive generations allow interconnect lengths and power dissipation to be reduced, MCMs will not have that same luxury. As the complexity of ICs advances, pinout count per IC increases, and operating frequencies increase, MCM normal metal interconnections will have to grow in length and will not be allowed to reduce in cross-sectional area. On MCM-D substrates, typical copper or aluminum interconnection dimensions are about 2 to 5 μm in thickness and between 15 and 30 μm wide with corresponding via sizes. By cooling the metal to 77 K (liquid nitrogen temperature), the resistivity of copper decreases by a factor of about 7 which allows a corresponding decrease in the interconnect's cross-sectional area. In order to increase the wiring density beyond that of cryo-cooled MCMs and improve the chip-to-chip bottleneck at high frequencies, alternatives to conventional metal interconnects must be considered [1].

HTS interconnections, with negligible resistivity at operating frequencies of several tens of GHz and lower, have great potential to reduce an interconnect's cross-sectional area with typical thicknesses of less than 1 μm and widths of less than 2 μm for MCM applications with similar spacings. The main challenge for attaining multiple layers of high density, high performance HTS interconnects appears to be in fabricating compact, low resistance vias.

The work presented here focuses on this problem and describes a method of fabricating noble metal vias for use in an HTS MCM prototype.

2. EXPERIMENTAL DETAILS AND RESULTS

A cross-section of our multilayer YBCO structure utilizing Au vias is shown in Figure 1.

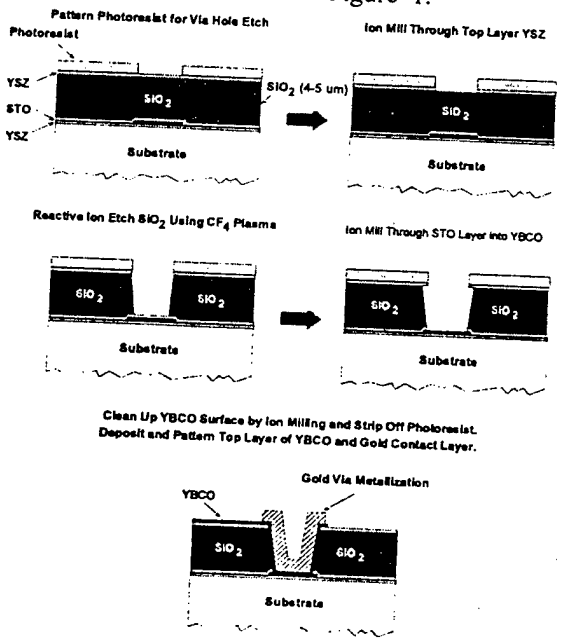

Figure 1. HTS via process.

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Our research has centered around two layers of laser ablated $YBa_2Cu_3O_{7-x}$ (YBCO) interconnects separated by a multilayer dielectric consisting of $SrTiO_3/SiO_2$/YSZ. We are able to attain critical current densities > 5 x 10^5 A/cm^2 in both YBCO layers. The $SrTiO_3$ (STO) and YSZ (yttria-stabilized zirconia) layers being ~0.5 μm thick while the SiO_2 ranges between 4 and 5 μm.

The via fabrication process is as shown in Figure 1. The etching involves a 500 eV ion mill through the top YSZ buffer layer, which is followed by a reactive ion etch through the SiO_2 interlevel dielectric selectively stopping at the barrier layer of STO. To complete the etching process, a 500 eV ion mill is done to etch through the STO. The final milling is very nonselective and requires close observation to keep from overetching through the bottom layer of YBCO. When depositing the top layer of YBCO at ~700° C, whatever material is deposited on the via sidewalls is presumably corroded due to interdiffusion of Si from SiO_2 into the YBCO but, presumably, does not effect the quality of the via. The subsequent *in situ* deposition of ~2000 Å of Au by laser ablation creates low resistance contacts without having to do a high temperature anneal in oxygen as was described by Ekin et al. [2]. In similar structures, contact resistivities of less than 10^{-7} Ω-cm^2 have consistently been attained. An additional 1.5-2.0 μm of Au is deposited over the existing YBCO/Au and then patterned using ion milling and photoresist as a mask.

This type of via structure has several advantages over previously demonstrated superconducting vias for use in HTS MCMs [3,4]. Since HTS thin films need to be deposited on planar surfaces or gradual slopes to maintain a reasonable current density, due to grain boundary problems, they require gradually sloped via holes that take up a wide area. By using a noble metal, compact, high-aspect ratio vias can be fabricated reliably.

Ultrasonic Al wire bonds were then made between YBCO/Au bond pads on the substrate and a wire bondable PC board. Via chain resistance was measured using a conventional 4-point contact configuration and measuring the voltage drop across the vias while passing DC current through it. The resistance vs. temperature of a ~0.5 cm long via chain structure with ten 40 μm square vias interconnecting 50 μm wide YBCO lines is shown in Figure 2. The room temperature resistance was measured to be about 515 Ω, and upon cooling to 78.5 K, the resistance

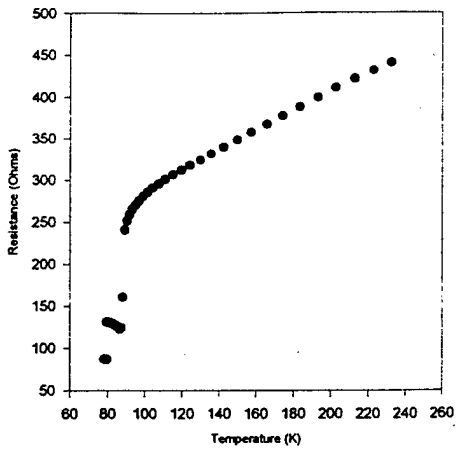

Figure 2. Temperature transition of a chain of ten 40 μm wide vias.

dropped to about 87 Ω. As is shown in Figure 2, there are two separate superconducting transitions occurring at about 89 K and 80 K which correspond to the top and bottom layer YBCO transitions. At 78.5 K, the interconnects had not yet become fully superconducting.

In summary, 40 μm YBCO/Au via chain structures have been characterized. The preliminary work shown here is to be improved upon by improving the quality of the YBCO layers, lowering the contact resistances, and possibly improving the step coverage of Au through the via by increasing its thickness.

ACKNOWLEDGEMENT

This work was supported in part by NSF (DMR 9318946), U.S. Army Research Office (DAAH04-96-1-0455), and DARPA (MDA 972-93-I-0036).

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PHYSICA

Fabrication techniques and electrical properties of $YBa_2Cu_3O_{7-x}$ multilayers with rf sputtered amorphous SiO_2 interlayers

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We have successfully fabricated $YBa_2Cu_3O_{7-x}$/YSZ/SiO_2/YSZ/$YBa_2Cu_3O_{7-x}$ multilayer structures on single crystal $LaAlO_3$ (100), substrates. The $YBa_2Cu_3O_{7-x}$(YBCO) layers were deposited using pulsed laser ablation (PLD), the biaxially aligned YSZ (250 nm thick) layers were deposited using ion beam assisted PLD (IBAD-PLD), and an amorphous SiO_2 (1-2μm) layer fabricated via rf sputtering was sandwiched between the YSZ layers. Fabrication techniques and characterization results are reported for patterned layers in this work.

1. INTRODUCTION

For high temperature superconductor multichip module(HTS-MCM) applications the basic building block is the HTS/Insulator (thickness >1μm)/HTS structure. A HTS-MCM can be defined as a miniaturized version of a multilayered printed wiring board with superconducting interconnects. Previously such a HTS-MCM prototype using a YBCO/$SrTiO_3$(500nm)/YBCO has been successfully fabricated by Burns et al [1]. Recently the use of ion beam assisted deposition to deposit biaxially aligned YSZ buffer layers on polycrystalline or amorphous substrates allowed for good quality YBCO films on these substrates [2-5]. Réade et al [6] were able to demonstrate using the ion beam assisted pulsed deposition (IBAD-PLD) technique that it was possible to fabricate the YBCO/YSZ-/amorphousYSZ(5μm)/YSZ/YBCO multilayers on oriented YSZ substrates with the top YBCO T_c ~ 87 K. They also fabricated the same structure using amorphous SiO_2, but cracks in the top YBCO layer did not permit electrical measurements of the top layer. The main advantage of SiO_2 is its low dielectric constant (~ 3.89), which makes it an ideal insulator material for MCMs.

In this paper we briefly describe the method to fabricate and the results obtained from the characterization of the YBCO/YSZ-/SiO_2/YSZ/YBCO multilayers.

2. EXPERIMENTS

The first YBCO layer (300nm thick) was fabricated by pulsed laser deposition using standard conditions. After patterning, part of the pads were masked to allow for transport measurements later. Next a 250 nm thick YSZ layer was deposited via IBAD PLD using conditions described in [5]. After this a 1-2 μm thick SiO_2 layer was deposited by reactively sputtering a Si target in oxygen ambient (the details of this process are described in [4]). Following the SiO_2 deposition another 250 nm thick biaxially aligned YSZ buffer/capping layer was deposited via IBAD PLD. Finally the masks were taken off and the top YBCO was deposited using the same conditions as the first YBCO except that the deposition temperature was kept ~ 20-30° lower. For the first set of multilayers the top YBCO layer was patterned into bridges over the underlying bridge patterns but shifted a little to the side so that the top bridge goes over step edges. The patterning was carried out by using photolithography and ion milling. For the second set of multilayers the top YBCO layer was patterned into

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bridges whereas the bottom YBCO layer was not patterned. Finally in the third set the top YBCO layer was patterned into serpentine (meander) lines crossing over the patterned bottom YBCO serpentine lines

3. RESULTS

The X-ray diffraction pattern for an unpatterned multilayer in Fig. 1. shows that the films have good *c*-axis orientation. We also measured the top YBCO ϕ scan full width at half maximum (FWHM) ~ 26° (for the (103) peaks), while for YSZ (111) peaks the FWHM was ~ 2-3° greater than that of the top YBCO.

For the first set, the bottom 40 μm wide bridge the T_c ~ 90 K and J_c ~ 2×10^6 A/cm² whereas for the top YBCO bridge 60 μm wide (with step edges), the T_c ~ 86-87 K and J_c ~ 3×10^4 A/cm². In the second set, the top YBCO bridge patterns of the same width without step edges the J_c ~ 10^5 A/cm² with Tc ~ 87-88 K. Finally in Fig. 2(A) is shown the resistance versus temperature plot for 20 μm serpentine bottom YBCO line 19 cm long the T_c ~87 K and J_c ~2×10^5 A/cm², whereas the same width serpentine line on the top layer showed semiconducting behavior as seen in Fig.2(B).

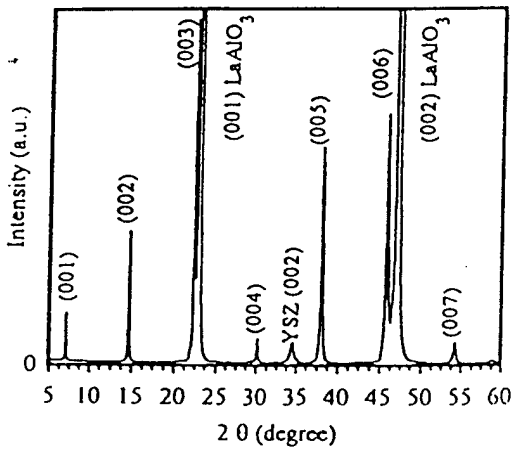

Fig. 1 X-ray diffraction pattern for a multilayer YBCO/YSZ/SiO_2/YSZ/YBCO sample

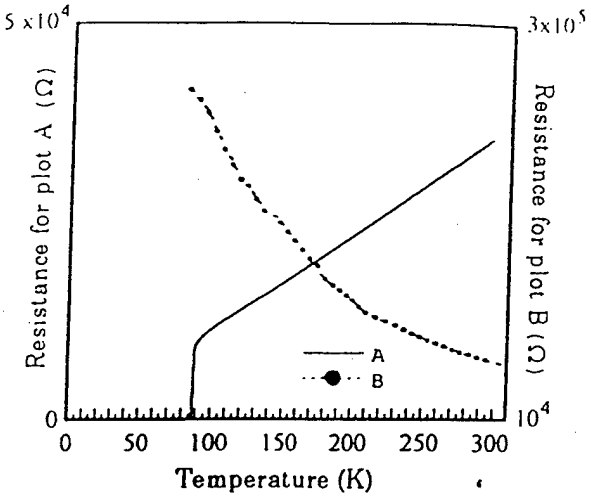

Fig. 2 Resistance versus temperature curves for (A) 20 μm wide bottom YBCO serpentine line. (B) 20 μm wide top YBCO serpentine line

4. CONCLUSIONS

Good quality YBCO layers separated by an amorphous SiO_2 interlayer have been fabricated by using biaxially aligned YSZ layers. However if the bottom YBCO is densely patterned then planarization is necessary to prevent degradation of superconducting properties at the step edges.

ACKNOWLEDGEMENT

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$Y_1Ba_2Cu_3O_{7-x}$ multilayer structures with a thick SiO_2 interlayer for multichip modules

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For high temperature superconducting multichip modules and other related electronic applications, it is necessary to be able to fabricate several $Y_1Ba_2Cu_3O_{7-x}$ (YBCO) layers separated by thick low dielectric constant dielectric layers. In this work, we report the successful fabrication of YBCO/YSZ/SiO_2 (1–2 μm)/YSZ/YBCO multilayer structures on single crystal yttria stabilized zirconia (YSZ) substrates. In contrast to previously reported work, the top YBCO layer did not show any cracking. This is due to a technique that allows for stress relief in the SiO_2 layer before the second YBCO layer is deposited. The top YBCO layer in our multilayer structure had T_c = 87 K and $J_c = 10^5$ A/cm^2 (at 77 K), whereas the bottom YBCO layer had T_c = 90 K and $J_c = 1.2 \times 10^6$ A/cm^2 (at 77 K). We also showed that the quality of the bottom YBCO layer was preserved during the fabrication of the multilayer due to the annealing process during which O_2 diffused into the YBCO, replacing the O_2 lost during the deposition of the top YBCO layer.

I. INTRODUCTION

In high temperature superconducting (HTS) multichip modules (MCM's) the basic building block is a multilayer structure consisting of several superconductive layers separated by thick dielectric layers. The HTSC layers are patterned into interconnects for electrically connecting the different chips on a layer, and vias are used for interconnecting the various YBCO layers. In order to keep the distributed capacitance low,[1] the thickness of the interlevel dielectric layer should be of the order of the HTSC interconnect line width and have a low dielectric constant (ideally <5). Such a multilayer structure would have a power plane, a ground plane, and two or more wiring layers.[1] However, by using the Interconnected Mesh Power System (IMPS) topology,[2] a superconducting MCM (IMPS-MCM) can be realized using only two layers of superconducting interconnects. Switching from a four-layered structure to one with only two layers greatly reduces the technological difficulties as well as cost. Previously reported work on multilayer structures used sputtering or pulsed laser deposition (PLD) at high temperatures (700–800 °C) in order to achieve epitaxial growth of the dielectric layer.[3–7] The main drawback with this process is the loss of O_2 from the underlying $Y_1Ba_2Cu_3O_{7-x}$ (YBCO) layer due to the long deposition time required in the case of thick dielectric layers. The loss of oxygen in the underlying YBC layer results in severe degradation of its superconducting properties.

Previously YSZ has been successfully used as an epitaxial buffer layer for depositing high quality YBCO films on technologically important substrates, such as SOS (Silicon on Sapphire) and Si.[8,9] In recent years the other major use of YSZ has been in the deposition of biaxially aligned YSZ buffer layers on amorphous or polycrystalline substrates, such as pyrex, Haynes alloy, and nickel.[10–15] The biaxially aligned YSZ layers are deposited at room temperature using the ion beam assisted deposition (IBAD) method.[12] These results therefore indicate that IBAD YSZ could be used for fabricating multilayers with amorphous isolation layer materials that have lower dielectric constants suitable for MCM applications. For example, YBCO/YSZ/SiO_2/YSZ/YBCO/YSZ (substrate) multilayer structures fabricated using the plasma enhanced chemical vapor deposition (PECVD) method for depositing the amorphous SiO_2 layer, and ion-beam assisted PLD for the biaxially aligned YSZ dielectric layers on single crystal YSZ substrates have previously been reported.[16] SiO_2 was chosen as the insulating layer because of its low dielectric constant ($\epsilon \sim 3.8$). Unfortunately, cracks in the top YBCO layer did not allow for transport measurements and pre-

vented applications of the multilayered structure, as reported in Ref. 16. In this paper, we describe a technique to produce two high quality YBCO layers and present results of transport T_c and J_c measurements for both YBCO layers in a YBCO/YSZ/SiO_2/YSZ/YBCO/YSZ (substrate) multilayer structure which make the possibility of a HTS-MCM a realizable goal.

II. EXPERIMENTAL

In our experiments the first 2500 Å thick YBCO layer was deposited on a 0.5″ × 0.5″ YSZ single crystal substrate using an ArF excimer laser (wavelength = 193 nm, frequency = 5 Hz). The beam was focused to an energy density of ~3–4 J/cm^2. Substrate temperature of 750 °C and an O_2 pressure of 200 mTorr were maintained in the deposition chamber. We used three YBCO targets mounted on a carousel. The targets were exposed alternately for 2 min, and the deposition rate was ~150 Å/min. We have found that this technique results in higher yield of good quality YBCO films as compared to the yield of good quality films using a single YBCO target. After deposition the chamber was backfilled with 500 Torr of O_2, and bottom YBCO film was cooled to room temperature in about 70 min. After this the YBCO film was polished in a slurry of isopropanol and CeO_2 polishing powder. This is an important step that reduces the average surface roughness of the YBCO film (from 16 nm to 3 nm) and the number of boulders on the surface.[17,18] A bridge (40 μm wide) was patterned using photolithography and ion milling. Part of the pads to the bridge were masked during the deposition of the next insulating layer so as to allow for transport measurements at the end of the multilayer fabrication.

The second layer of 2500 Å thick YSZ was then deposited using ion-beam assisted PLD.[16] This layer serves as a capping layer to prevent diffusion of the (to be deposited) amorphous SiO_2 layer (3rd layer) into the YBCO layer. Diffusion of SiO_2 into the YBCO layer has been observed to have an adverse effect on the YBCO film properties.[19–23] We used a biaxially aligned YSZ layer because some samples fabricated with an amorphous YSZ layer resulted in poor quality bottom YBCO layers. This could be due to the less dense structure of amorphous YSZ, allowing for diffusion of SiO_2 through the YSZ capping layer and into the underlying YBCO layer.

The samples were then transferred to a PECVD system for deposition of a 1–2 μm thick SiO_2 layer. Our first attempts at depositing PECVD SiO_2 at 250 °C and an rf power of 55 W resulted in cracking of the multilayers during the deposition of the top YBCO layer, as reported by Reade *et al.*[16] In order to determine at which step in the process of making the multilayered structure cracking occurs, we stopped before adding the SiO_2 layer. Next the YSZ/YBCO/YSZ (substrate) structures were heated to 450 °C for 10 min in 500 Torr of O_2. Parts of these test samples were heated to 450 °C in vacuum. Most of the samples did not crack except for very few cases where cracks would appear in the YSZ layer, especially if prior to YSZ deposition the patterned YBCO samples were left exposed to ambient conditions (relative humidity ~50%) for long periods of time.

Next, to determine whether cracking was due to stress in the PECVD deposited SiO_2, we heated SiO_2/YSZ/YBCO/YSZ (substrate) structure in vacuum soon after depositing the PECVD SiO_2. Here we found that small islands of all three layers begin to peel off the substrate at about 300 °C, thus suggesting that the stress which leads to cracking originates from the SiO_2 film. In order to overcome the cracking problem in the case of PECVD deposited SiO_2, we followed procedures based on earlier work done on PECVD and CVD SiO_2 layers deposited on silicon substrates.[24–30] Evidence offered in previous work indicates that PECVD SiO_2 is in tensile stress before annealing. Annealing the SiO_2 in a N_2 ambient at high temperatures (>700 °C) reduced the water and silanol content, increased the density, and decreased the tensile stress. Instead of annealing in a N_2 ambient, we observed that if the SiO_2 layers were heated (ramp up ~10 °C/min) in 500 Torr of O_2 and annealed for ~8 min at 650 °C, no cracks were present during the later stages in the multilayer fabrication. This success is likely to be due to the reduced tensile stress in the SiO_2 after annealing. As a result after annealing, heating of the SiO_2 layer during the deposition of the top YBCO will no longer increase the tensile stress beyond the cracking point. The above annealing step allowed for successful fabrication of the entire multilayer. Samples annealed at temperatures below 650 °C still exhibited cracks as before.

After annealing, the SiO_2 layer was again capped with a 2500 Å thick biaxially aligned YSZ layer (4th layer), which also serves as an epitaxial template for the topmost YBCO layer. Finally, the 2000–2500 Å thick top YBCO layer (5th layer) was deposited under the same conditions as the first YBCO layer except that after pumping the chamber down to a base pressure of 5 × 10^{-5} Torr, it was immediately back-filled with 500 Torr of O_2, and then the substrate was heated to ~630 °C. As soon as the substrate temperature reached 630 °C the chamber was again pumped down to 200 mTorr for the YBCO deposition at 720 °C. This approach minimizes the degradation of the bottom YBCO layer. This is indicated by the fact that in the case of samples where the top YBCO layer was fabricated under the same conditions as that of the bottom layer, we observed a degradation in both the T_c values and J_c values of the bottom YBCO layer.

III. RESULTS AND DISCUSSION

The orientation of the YSZ and YBCO layers was characterized by x-ray diffraction. The x-ray diffraction pattern for the multilayer structure shown in Fig. 1 indicates good *c*-axis orientation. The ϕ scan widths (FWHM) for the top layer YBCO (103) were 26°–28°. For both the top and bottom 2500 Å thick IBAD-YSZ layer the ϕ scan widths (FWHM) obtained is ~32°. The in-plane alignment achieved using IBAD is independent of the template used. Better in-plane alignment of the top IBAD YSZ layer can be achieved by increasing its thickness. For example, a 5000 Å thick YSZ layer has a ϕ scan width of 24°, as reported in Ref. 31.

A schematic of the patterned layers used for the transport measurements is shown in Fig. 2. The bottom layer consists of a 40 μm wide bridge [Fig. 2(a)], as well as an unpatterned part of the bottom layer [Fig. 2(b)] to provide a comparison between the T_c and J_c values of the top layer bridges with and without step edges [Figs. 2(c) and 2(d), respectively]. All the transport measurements were obtained using the four-probe method.

Figure 3 A shows the resistance versus temperature curve for the 40 μm wide bottom YBCO bridge. Its T_c was 90 K and its $J_c = 1.2 \times 10^6$ A/cm^2. The top layer 60 μm wide bridge with step edges had T_c = 87 K (Fig. 3 B) and $J_c = 4.5 \times 10^4$ A/cm^2. The 30 μm bridge without step edges had the same T_c value (Fig. 3 C), but its J_c was 1×10^5 A/cm^2. The reduced critical current for the 60 μm bridge with step edges could be attributed to disruption of epitaxial growth at the step edges and large-angle grain boundaries.[1,32] No shorts were detected between the top and bottom YBCO layers from electrical resistance measurements. In addition, our experiments on YBCO/YSZ/SiO_2/YSZ/YBCO/YSZ (substrate) multilayered structure have consistently shown that the magnetic field dependence of

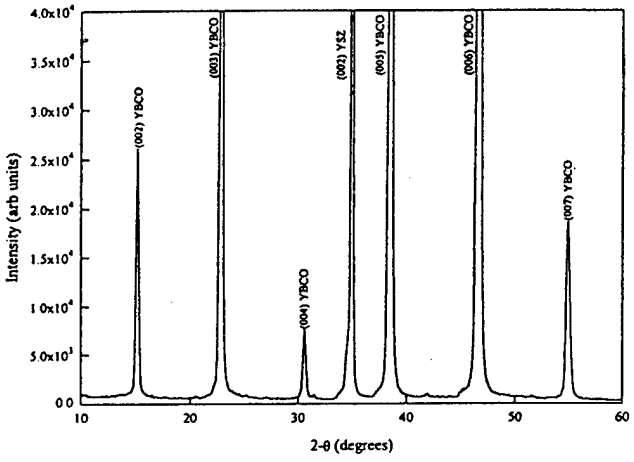

FIG. 1. θ-2θ x-ray diffractometer pattern for the YBCO/YSZ/SiO_2/YSZ/YBCO structure on (001)YSZ.

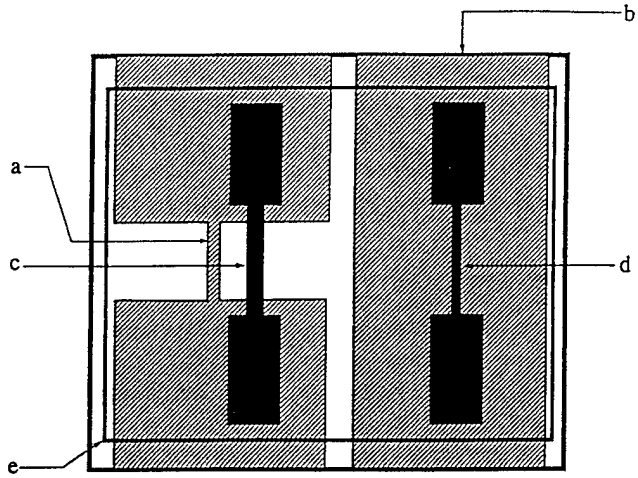

FIG. 2. Schematic of the patterned multilayer structure. (a) 40 μm wide bridge in the bottom YBCO layer. (b) Unpatterned bottom YBCO layer. (c) 60 μm wide bridge with step edges on the top YBCO layer. (d) 30 μm wide bridge without step edges on the top YBCO layer. (e) YSZ/SiO_2/YSZ insulator layers.

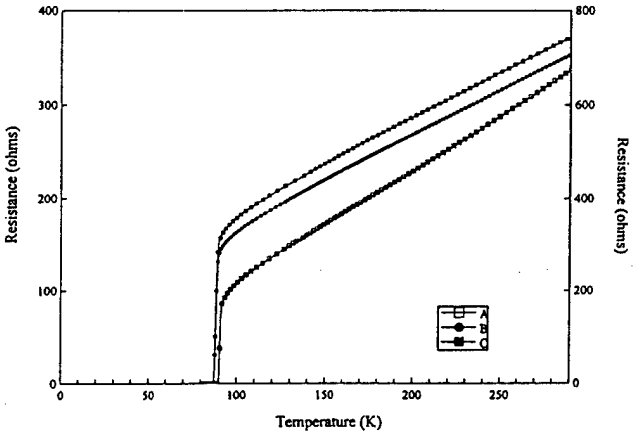

FIG. 3. Resistance versus temperature for the (A) 40 μm wide bridge in the bottom YBCO layer. (B) 60 μm wide bridge in the top YBCO layer with step edges. (C) 30 μm wide bridge in the top YBCO without step edges. Left *y*-axis used for plots A and C and right *y*-axis for plot B.

J_c is not appreciably altered over that of a single layer YBCO film. For example, we have found that for the multilayered structures, the J_c of the top layer was 1×10^4 A/cm^2, measured using the magnetization method at 77 K in a field of 1 T (magnetic field applied parallel to the *c*-axis). This number is consistent with what others have reported for a single layer on a polycrystalline substrate with an IBAD YSZ buffer layer.[12] For the bottom layer the J_c was 5×10^4 A/cm^2 at 77 K in a field of 1 T (magnetic field applied parallel to the *c*-axis).

Studies carried out on YBCO/epitaxial insulator bilayers[3] showed a significant decrease in the O_2 diffusion rate due to the presence of the epitaxial insulating layer.

In order to investigate the effect of YSZ/SiO_2/YSZ layers and the effect of the top YBCO layer deposition on the underlying YBCO layer, we patterned a 40 μm wide bridge on the bottom YBCO. Next, we deposited the YSZ/SiO_2/YSZ layers; measurements performed after this step were $T_c \sim 90$ K (Fig. 4 C) and $J_c \sim 1.0 \times 10^6$ A/cm^2. Thereafter we simulated the top YBCO layer deposition, except that no top layer was deposited and the YSZ/SiO_2/YSZ/YBCO structure was cooled down immediately (~15 min) in 200 mTorr of O_2. The resistance versus temperature curve (Fig. 4 A) shows a twentyfold increase in the bridge resistance at room temperature and the bridge is no longer superconducting. After these measurements the structure was annealed at 450 °C in 500 Torr of O_2 for 30 min. The results of T_c (Fig. 4 B) and J_c measurements showed no appreciable change as compared to the original values, indicating that the superconducting properties were entirely recovered. Thus we have demonstrated that during the top YBCO layer deposition, O_2 diffuses out of the underlying YBCO layer resulting in a tetragonal YBCO, while annealing in 500 Torr of O_2 results in rediffusion of O_2 which returns it back to the orthorhombic structure. The above results indicate that O_2 readily diffuses through the thick YSZ/SiO_2/YSZ interlevel dielectric. Efforts are currently underway to estimate the diffusion constant for O_2 through the YSZ/SiO_2/YSZ structure.

IV. CONCLUSION

We have reported on an investigation of the development of a structure that has potential to lead to a HTS MCM. Our results demonstrate that stress relief in PECVD deposited SiO_2 via an annealing process can avoid cracking in this multilayer structure. We have also demonstrated that YSZ/SiO_2/YSZ multilayer structure is a good O_2 diffuser. Although the total thickness of the YSZ/SiO_2/YSZ multilayer structure is ~2–3 μm, a sufficient amount of O_2 can still diffuse into the bottom YBCO layer in a relatively short time. By achieving better in-plane alignment for the IBAD YSZ layer, the top layer J_c can be further improved. Also, lower J_c values obtained in the case of a top layer bridge with step edges clearly indicates the need for planarization. We are currently working on improving the top YBCO layer J_c and are developing a planarization process.

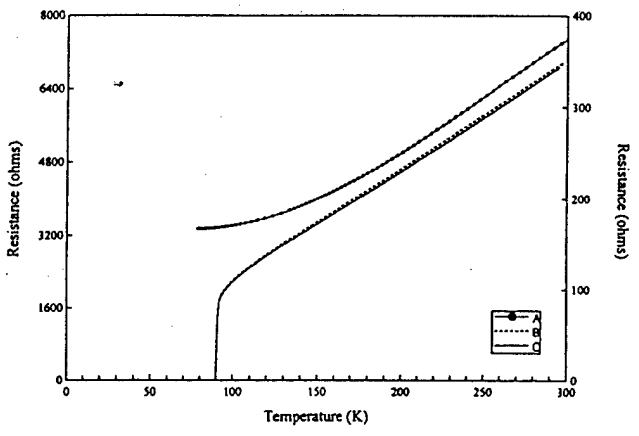

FIG. 4. Resistance versus temperature for the 40 μm wide bridge in the bottom YBCO. (A) After simulation of top YBCO deposition. (B) After annealing at 450 °C in 500 Torr of O_2 for 30 min. Left y-axis used for plot A and right y-axis used for plots B and C. (C) Before simulation of top YBCO deposition.

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Presentation

A Comparison of High-Temperature Superconductors in Multi-Chip Module Applications

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Abstract

In the application of high-temperature superconductors (HTSCs) in multi-chip module (MCM) technology, it is first necessary to investigate the advantages and disadvantages of the various HTSC compounds. The standard criteria for comparing the suitability of HTSCs in electronics applications has been critical temperature (T_c) and critical current density (J_c). It is also necessary to consider the physical properties of HTSCs in relation to the various processing techniques required in fabrication of MCMs. These techniques can be grouped into four main areas: deposition, patterning, packaging, and characterization. The four main HTSC materials, Y-Ba-Cu-O, Bi-Sr-Ca-Cu-O, Tl,Ba-Ca-Cu-O and Hg-Ba-Ca-Cu-O, will be compared to determine which is most suitable for MCM application.

Introduction

In the decades since the popular advent of the transistor in the 1960s, there has been continual and steady improvement in both the performance and cost of electronics equipment through miniaturization. This effort has given us the multi-chip module (MCM) as the latest and most promising technique to be introduced. MCM technology improves the speed at which devices can operate and decreases the power lost by eliminating as much length as possible from the interconnection between the individual devices. With this new technology some new barriers to increased speed and performance have arisen. By concentrating all of the devices in one area, the problems due to Joulean heating (I^2R losses) and electromigration are increased. Also, the lack of recent improvements may indicate that the upper limit of the speeds that can be expected from current semiconductor devices using conventional interconnects have been reached.

All of these problems can be addressed by combining high-temperature superconductors (HTSCs) with MCMs. Some of the interconnecting lines may typically carry 50 - 100 mA of current. Therefore, they account for a major portion of the heat generated (Burns et al., 1993). Replacing the lines with zero resistance HTSCs eliminates these I^2R losses. This means less heat and less power consumed. The refrigeration required for HTSC operation further limits the overall heat production to less than that produced by the individual devices. All of this allows for an even greater decrease in the interconnection lengths which, in turn, maximizes the operating speed of the MCM.

HTSC devices have been shown to be more than 2.5 times faster than their semiconductor counterparts, use three orders of magnitude less power, and do not suffer from electromigration problems (Van Duzer and Tuner, 1981). Their use in MCMs should produce the next quantum jump in performance. A cross-sectional schematic of an MCM is shown in Figure 1.

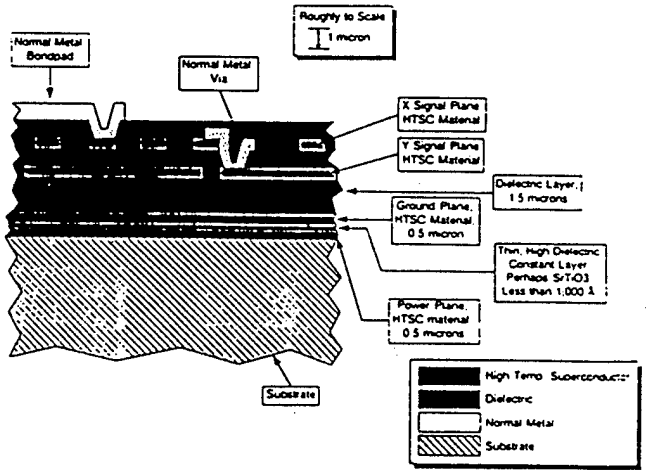

Fig. 1. Cross-sectional Schematic of a Superconducting Multi-Chip Module.

But, which HTSC offers the best overall prospects for MCM applications? This is the first question to be answered in the search for a viable superconducting MCM. When comparing HTSCs, the standard for suitability in electronics applications has been the materials critical temperature, (T_c), and critical current density, (J_c). It is

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APRIL 8-9, 1994

Gamma-ray and Fast Neutron Radiation Effects on Thin Film Superconductors*

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Abstract

The gamma-ray and neutron radiation hardness of $YBa_2Cu_3O_{7-x}$, $Tl_2Ba_2CaCu_2O_{8+x}$, and $Tl_2Ba_2Ca_2Cu_3O_{10+x}$ superconducting thin films deposited by off-axis sputtering and laser-ablation deposition techniques on substrates of MgO and $LaAlO_3$ was investigated. The unbiased samples were irradiated with 662 keV gamma-rays up to a cumulative dose of 1.5 Mrad(Si) and with neutron fluences up to 1×10^{14} neutrons/cm^2.

It was determined through nondestructive critical temperature transition, T_c, and critical current density, J_c, measurements and x-ray diffraction analysis that the thin film superconductors were radiation hard up to moderate levels of neutrons and gamma-rays. It was also determined that extended exposure to moderately humid air degraded the critical current density of all the films.

I. Introduction

Space applications of multichip modules (MCMs) appear to be part of the driving force for their development. In the future, thin film superconductors (TFSCs) will potentially be used as interconnects for MCMs. As a result of this application of TFSCs, their response to a radiation environment is of great interest. In the past, studies of radiation effects on superconductor materials have been restricted to the bulk form [1-5], but if superconducting interconnects are to be used in future MCMs, the impact of exposure to gamma-rays and fast neutrons on the properties of TFSC materials must be examined. In addition to the effects of radiation on the superconductor material, the substrate material on which the superconductor is deposited, as well as the dielectric material used to separate the multiple levels of interconnects, must also be examined for sensitivity to radiation exposure.

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II. Experimental Procedures

In the work reported here, $YBa_2Cu_3O_{7-x}$ (YBCO), $Tl_2Ba_2CaCu_2O_{8+x}$ (Tl-2212), and $Tl_2Ba_2Ca_2Cu_3O_{10+x}$ (Tl-2223) thin films on substrates of MgO and $LaAlO_3$, some of the more common superconductor/substrate combinations, were subjected to both gamma-ray and neutron radiation in an electrically unbiased state. Although radiation without bias does not fully explore the impact on dielectric substrates, it does examine the impact on high temperature superconductors. The samples were deposited using laser-ablation and off-axis sputtering techniques, and were of varying quality and thickness in order to determine if their radiation hardness varied accordingly. The thin film thicknesses ranged from about 200 to 1000 nm.

The superconductors were characterized by their critical temperature transition, T_c, and critical current density, J_c, measured using a nondestructive inductance method as described by Claassen et al. [6]. This measurement technique involves placing a thin, multiturn copper coil next to the film surface and driving the coil with a low distortion audio-frequency sine-wave current. In turn, the driving current induces shielding currents in the film. The nonlinearity in the coil-film system increases abruptly when the induced current in the film reaches its critical level. A schematic of the measurement system used is shown in Figure 1. The resulting voltage across the coil is filtered by a passive twin-tee notch filter with a center frequency the same as the drive current frequency, 1 kHz, and analyzed by the lock-in amplifier for third harmonics. Either a single or double coil can be used. A single coil acts as "both the drive and pickup coil." We have used a single coil setup in our measurements since it functions as well as a two coil setup according to Claassen et al. The samples were measured down to liquid nitrogen temperature (77 K). This type of measurement was chosen over the four point contact method because the samples had to be measured after each irradiation. Any probe technique would destroy a large surface area of the film after each subsequent measurement since we were dealing with samples less than 1 cm^2. A Philips x-ray diffractometer was also used in an attempt to detect any atomic disorder in the superconductor films resulting from neutron bombardment.

The superconductor/substrate structures were irradiated with gamma-rays up to a cumulative dose of 1.5 Mrad(Si)

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Title of Paper: Development of vias for use in high temperature superconductor multichip modules

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In the development of high speed multichip modules, high temperature superconducting interconnects are viewed as a viable alternative to copper interconnects to improve the overall speed of the module. Vias that provide low contact resistivity connections to the superconducting layers while maintaining space efficiency and fabrication compatibility are necessary for efficient utilization of the superconductors. Our research involves the fabrication and characterization of noble metal (primarily Au and Ag) vias to connect multiple layers of YBCO interconnects.

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Ion Beam Assisted Sputter Deposition of CeO_2 Buffer Layers for Superconducting Multichip Module (MCM) Applications

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Cerium dioxide (CeO_2) buffer layers have been sputter deposited onto various substrates including silicon and nickel alloy using ion beam assisted deposition (IBAD). This technique has resulted in the formation of CeO_2 which exhibits strong (100) phase growth as well as in-plane orientation as evidenced by X-ray diffraction. Subsequent YBCO depositions on these films exhibit T_c's of 86 K and biaxial texture with the c-axis normal to the surface. With further refinement, this technique may be used to fabricate the multilayer structure needed for superconducting multichip modules.

INTRODUCTION

There is widespread interest in the use of superconducting interconnects in electronics, especially in multichip modules (MCMs). Superconductor interconnects have advantages of low signal loss and very low RC propagation delays. Furthermore, due to the reduction in interconnect resistance, the linewidths can be made much smaller, allowing for a reduction in the number of signal layers. One proposed structure for the superconducting MCM is the interconnected mesh power system (IMPS), which requires only two interconnect layers, thereby reducing the complexity of the manufacturing process (1). In order to achieve satisfactory electrical performance and reduce parasitic capacitances, these interconnects need to be separated by a thick (~2-5 μm) insulating layer with a low dielectric constant. Possible substrate and dielectric materials for these applications include silicon, silicon dioxide, or other polycrystalline materials. However, it has been shown that YBCO deposited directly onto these materials reacts with them and degrades the YBCO superconducting properties. The use of buffer layers such as cerium dioxide (CeO_2) or yttria-stabilized zirconia (YSZ) can mitigate these problems, but they have high dielectric constants and need to exhibit a high degree of biaxial texture to reduce high-angle grain boundaries and improve the critical current density, J_c, of the YBCO layer.

One possible interconnect structure that has been proposed by researchers at the High Density Electronics Center (HiDEC) consists of two YBCO layers separated by a thick layer of SiO_2, which exhibits a low dielectric constant. To prevent interdiffusion and provide for an epitaxial surface on which high quality YBCO can be deposited, the SiO_2 is

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separated from the YBCO by a thin buffer layer of either cerium dioxide or yttria-stabilized zirconia. Clearly, the ability to deposit aligned buffer layers on polycrystalline or amorphous substrates would greatly improve the manufacturability of superconducting MCMs.

Ion beams have been used previously to deposit aligned buffer layers for YBCO on polycrystalline substrates. Iijima *et al.* (2) reported a dual-ion beam process for depositing YSZ on Hastelloy C276, a nickel-based alloy. The ion beam position with respect to the substrate normal was varied from 30° to 60°, with bi-axially oriented films obtained at an angle of 45°. Reade *et al.* (3) also reported biaxial deposition of YSZ on nickel alloys when using ion beam assisted deposition in conjunction with laser ablation. The degree of orientation of the films was found to be strongly dependent on the incident angle of the ion beam, with the optimal results occurring at 55° from the substrate normal. Ion beam voltage and current also played important roles in determining the amount of orientation of the film. Oriented YSZ growth on Pyrex substrates using IBAD has also been reported by Sonnenberg *et al* (4). They reported detailed microstructural characterization, but did not subsequently deposit YBCO on these films. This paper reports our progress to date in the use of IBAD with magnetron sputtering, which has the advantage of producing larger area films than laser ablation.

EXPERIMENTAL DETAILS

All of the buffer layer films were deposited by RF magnetron sputtering in a deposition system designed at the University of Arkansas for superconductor and related dielectric research. Briefly, it is a 22" diameter side-sputtering deposition system that is pumped with two cryopumps. The deposition pressure can be precisely controlled from high vacuum to above 1 Torr, independently of the amount of backfill gas present. This is achieved through the use of separate high- and low-conductance paths to the cryopumps. Both conductance paths utilize servo-controlled throttle valves to maintain a constant pressure regardless of the gas flow present. The chamber has multiple ports for mounting two sputter guns, an ion beam, and two substrate holders, which also serve as heaters. The chamber was pumped down to 4×10^{-7} Torr before each deposition.

The ion beam used in these experiments is an Anatech IS-3000 3" filamentless gun. It was positioned about 8 cm from the substrate and at an angle of 55° from the substrate normal. This corresponds to the angle of the [111] direction from the [100] direction for cubic CeO_2, and it is believed that ions directed at this angle may suppress growth of the (111) phase while enhancing growth of the (100) phase (3). Argon gas was flowed through the gun and an acceleration potential of 200-300 eV was used, with a beam current of 2-5 mA.

The dielectric films were deposited from a stoichiometric 2" diameter CeO_2 target which was RF sputtered in 80% Ar and 20% O_2 at pressures ranging from 0.2 mTorr to 1 mTorr, and at power levels from 60-80 watts. The low pressures were required to create

a long enough mean free path for the ion gun to maintain a collimated beam. According to basic vacuum theory, a mean free path of 8 cm requires a pressure lower than 0.61 mTorr. Special modifications were made to the sputtering guns to allow them to maintain plasmas at such low pressures. These modifications basically consisted of flowing the sputtering gas inside the dark space shield of the sputter guns, creating a localized high pressure region. The substrate was unheated, but its temperature generally increased to about 50 °C due to radiative heating from sputtering and the ion beam.

The YBCO films were deposited in the same system described above, using a 2" magnetron sputtering gun in an off-axis geometry; the parameters are described elsewhere (5). Briefly, substrates were mounted onto a heater block using silver paste. The deposition temperature was held at 735 °C in 80% Ar and 20% O_2. After deposition, the samples were cooled in 700 Torr of oxygen.

The following substrates were used in this experiment: pieces of <100> prime silicon, 1" square Corning 7059 borosilicate glass (Pyrex), and 0.5" square Haynes alloy (#230). Haynes alloy is a nickel-based stainless steel which is a candidate substrate for YBCO films because of its low thermal expansion coefficient mismatch with YBCO. The Haynes alloy was mechanically polished using successively finer diamond paste to 0.25 μm. The three different materials represent crystalline, amorphous, and polycrystalline structures, respectively, and provide a thorough test of the ability of IBAD to deposit oriented films independently of the substrate structure or orientation.

Cerium dioxide films were deposited on the above substrates both with and without IBAD. All of the films in this study were grown to a thickness of about 2000 Å. The use of IBAD caused a decrease in the deposition rate, from about 16 Å/min to 13 Å/min. After all of the CeO_2 depositions were completed, the CeO_2 sputtering gun was removed and replaced with the YBCO sputtering gun. The CeO_2 films were removed for analysis, then remounted to the heater block for YBCO deposition. YBCO films of approximately 3500 Å thickness were deposited on the glass and Haynes substrates.

The thickness and index of refraction of the CeO_2 films deposited on bare silicon were measured using an ellipsometer. The structure of the films was analyzed with a Phillips PW-1830 four-circle x-ray diffractometer (XRD) using copper kα radiation, and the surface analysis was performed with a Digital Instruments atomic force microscope (AFM). Electrical characteristics were measured using a non-contact technique similar to the system described in (6).

RESULTS AND DISCUSSION

The index of refraction of both the IBAD and non-IBAD films was around 2.3, compared to 2.2 for bulk CeO_2. This indicates that the films are slightly oxygen deficient (7), but theta-two theta XRD scans show only evidence of the CeO_2 phase. The theta-two theta scan of CeO_2 on a silicon substrate without using IBAD is shown in figure 1. The presence of the (111), (200), and the (220) peaks are present at roughly the same

intensity, with the ratio of the (200) peak intensity to (111) peak intensity equal to 0.95. This suggests a polycrystalline film with no prevalent texture. The film consists of completely random oriented grains since the substrate does not provide epitaxy for the growing layers. Figure 2 shows the theta-two theta scan of CeO_2 on silicon using IBAD. As the figure indicates, IBAD causes a marked improvement in the texturing of the (100) phase. The other phases are significantly attenuated, with the ratio of (200) to (111) intensities equal to 14.5. One reason for this dramatic improvement in texture, besides the fact that IBAD was used, is that silicon is crystalline with very nearly the same lattice constant as CeO_2.

Figure 3 shows a theta-two theta XRD scan of IBAD deposited CeO_2 on Pyrex. While the (111) and (220) peaks are still visible, the (200) peak is dominant; the ratio of (200) to (111) intensities is 1.4. Figure 4 shows a phi scan of the (111) family of CeO_2 peaks on Pyrex and indicates both in-plane and out-of-plane orientation, as evidenced by the four peaks spaced 90° apart. The full-width-at-half-maximum (FWHM) for these peaks is approximately 34°. The relatively high FWHM implies that some in-plane misorientation is present. A theta-two theta scan of YBCO/CeO_2/Pyrex is presented in figure 5. Only c-axis YBCO growth is detected, which suggests that the CeO_2 deposition provides a well-aligned layer upon which the YBCO can be deposited. As a further demonstration of the alignment, figure 6 shows a phi scan of the YBCO (103) family of peaks with a FWHM of 22°. This indicates well-aligned grains in the a-b plane, which is parallel to the substrate. The presence of 45° misaligned grains would be indicated by peaks spaced 45° out of phase from the major peaks. Misaligned grains greatly reduce the J_c of the films.

Next, data for CeO_2 and YBCO/CeO_2 structures deposited on Haynes alloy are presented. Figure 7 shows a theta-two theta scan for CeO_2 deposited without IBAD. In this case, the CeO_2 peaks are barely discernible above the noise of the substrate, with the (111), (200), and (220) peaks at about equal intensity. The ratio of (200) to (111) intensities is equal to 0.9. Figure 8 illustrates a theta-two theta scan of YBCO deposited on Haynes alloy with an IBAD-deposited CeO_2 buffer layer. As in figure 5, only c-axis YBCO growth is evident. In addition, the (200) peak of CeO_2 is 3.2 times more intense than the (111) peak.

YBCO was deposited on the three CeO_2/substrate structures and their T_cs and J_cs were measured. T_cs (zero resistance) were 86 K, and J_cs ranged from 1×10^5 A/cm^2 to 5×10^5 A/cm^2 when measured at 77 K. These values are somewhat lower than T_cs and J_cs obtained for films deposited on single crystal substrates, such as yttria stabilized zirconia. The cause for the reduction in J_c is most likely due to the presence of high-angle grain boundaries, which are evident from the scan shown in figure 6. These grain boundaries are known to act as weak links and reduce the critical current density (8).

It is not well understood how the ion beam provides oriented film growth, but three separate mechanisms have been postulated. First, the collimated ion beam may selectively sputter grains growing in undesirable directions. Second, the beam is believed

to enhance film growth corresponding to the channeling direction of the film. As mentioned above, the [111] channeling direction is 55° away from the [100] direction. Therefore, a beam directed at this angle allows the (100) phase to become channeled to the growing film, while other phase growth is attenuated or slowly sputtered away. Finally, the ion beam imparts energy to the surface of the film, which provides increased mobility for the molecules to realign into the preferred orientation.

The average roughness R_a of the IBAD films was measured by AFM and found to be about 2.6 nm, while the R_a of the non-IBAD films was about 3.8 nm. This improvement in smoothness is most likely due to the tendency of the ion beam to etch peaked surfaces more rapidly than smooth areas (9). This enhances superconductor quality by providing a smooth surface for YBCO nucleation. The improved surface quality, along with the stronger presence of the (100) phase, is believed to be responsible for higher YBCO film quality.

CONCLUSIONS

Cerium dioxide films have been sputter deposited onto several substrate materials using IBAD. These films exhibit bi-axial alignment with dominant (100) phase growth, as indicated by XRD theta-two theta and phi scans. The argon ion beam was positioned 55° from the substrate normal. This angle corresponds to the angle of separation of the [111] direction of cubic CeO_2 from the [100] direction.

High quality YBCO was deposited over the IBAD buffer layers. The YBCO exhibited T_cs around 86 K and J_cs ranging from 1×10^5 A/cm^2 to 5×10^5 A/cm^2. IBAD has been shown to be a useful technique for depositing aligned films on crystalline, polycrystalline, and amorphous substrates. This capability allows greater flexibility in manufacturing superconductor-dielectric structures by enabling the use of low-cost substrates in place of lattice-matched single crystal substrates, which tend to be expensive, brittle, and have high dielectric constants.

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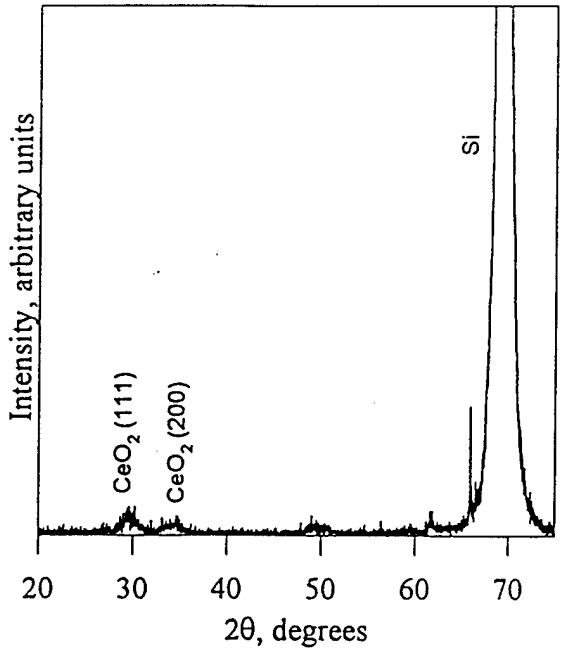

Figure 1. XRD scan of CeO_2 deposited on Si without IBAD.

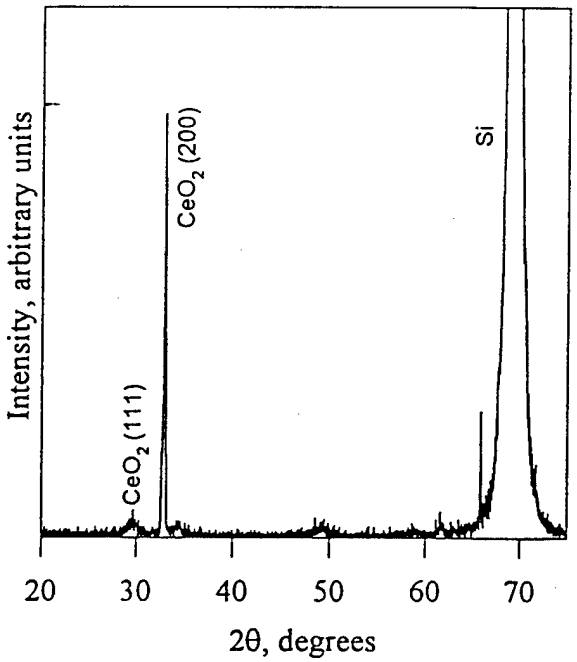

Figure 2. XRD scan of CeO_2 deposited on Si with IBAD.

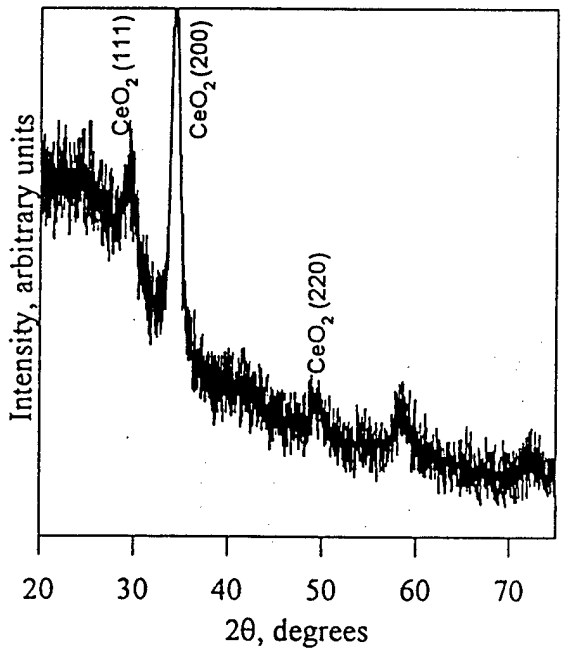

Figure 3. XRD scan of CeO_2 deposited on Pyrex with IBAD.

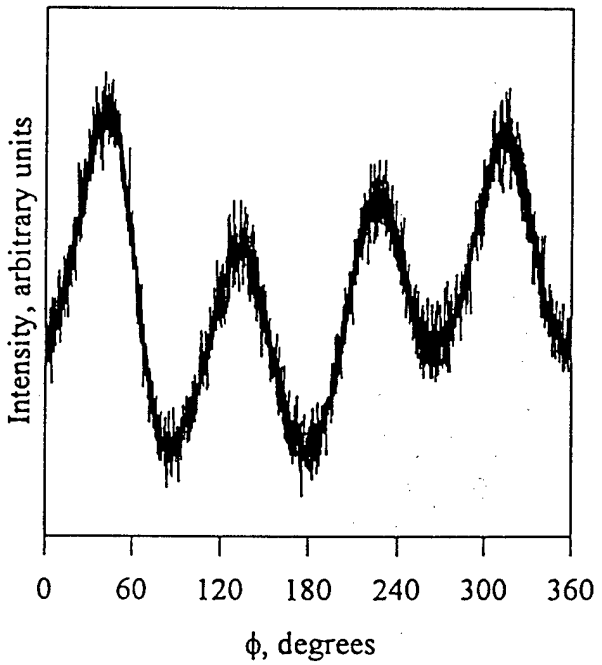

Figure 4. Phi scan of $CeO2_2$ (111) family of peaks deposited on Pyrex.

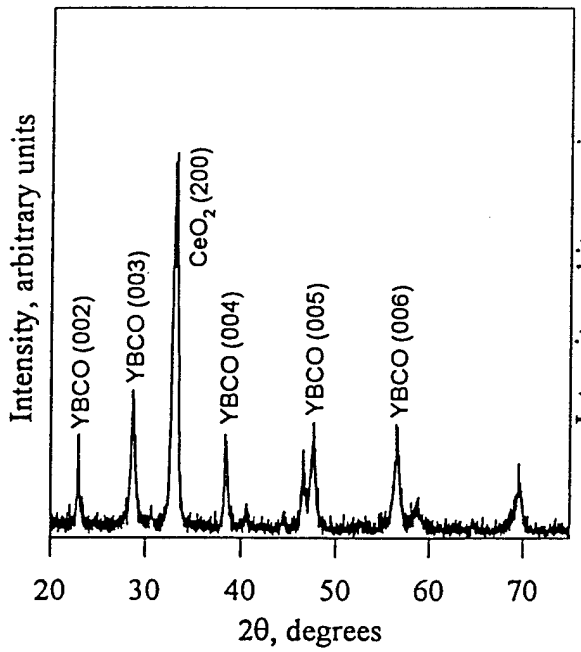

Figure 5. XRD scan of YBCO/CeO_2 deposited on Pyrex with IBAD.

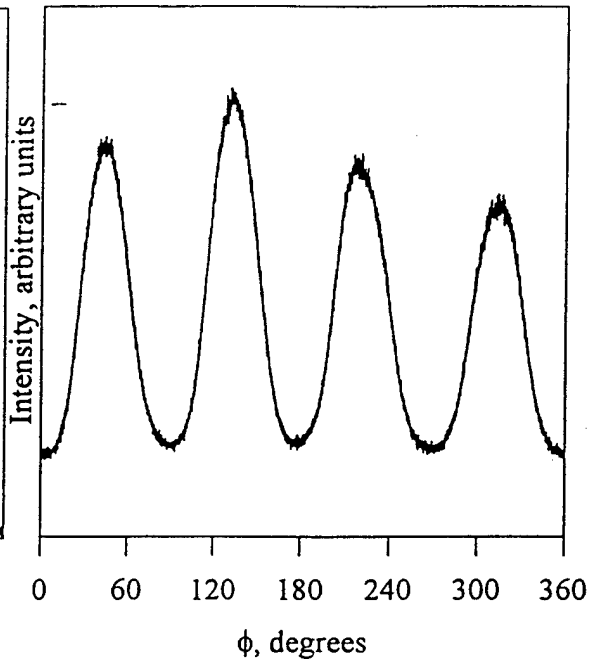

Figure 6. Phi scan of YBCO (103) family of peaks on CeO_2/Pyrex.

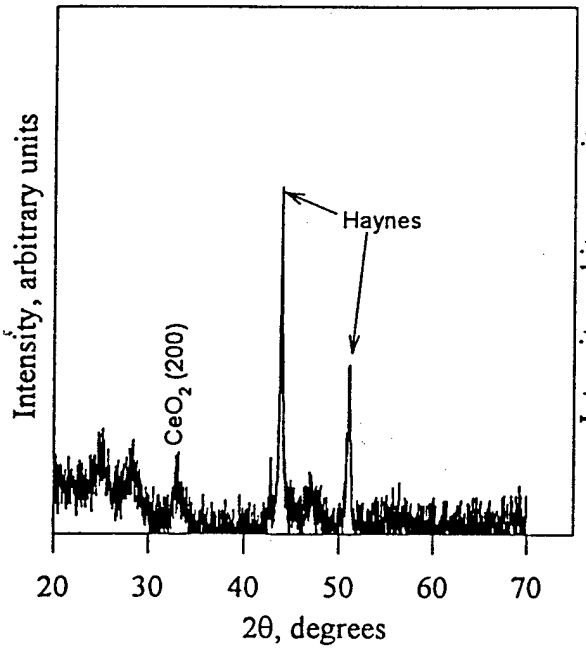

Figure 7. XRD scan of CeO_2 deposited on Haynes without IBAD.

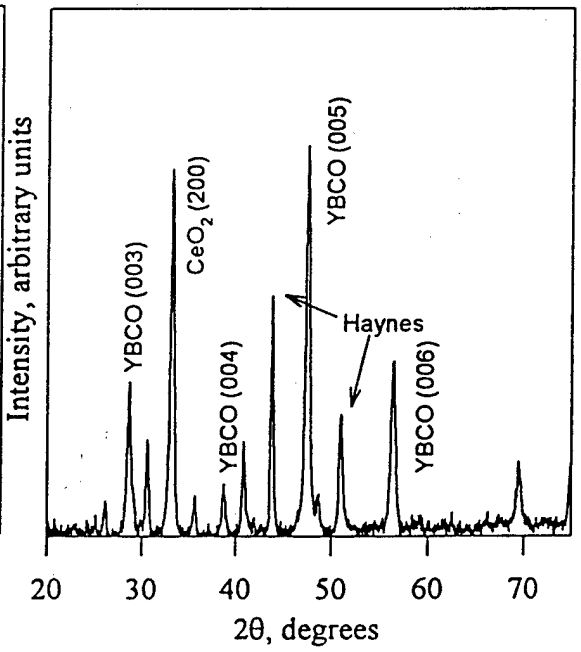

Figure 8. XRD scan of YBCO/CeO_2 deposited on Haynes with IBAD.

Ion Beam Assisted Sputter Deposition of CeO_2 Buffer Layers for Superconducting Multichip Module (MCM) Applications

List of Keywords

cerium dioxide
multichip modules (MCMs)
buffer layers
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sputtering
YBCO thin films
x-ray diffraction

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THE EFFECTS OF LOW-ENERGY BLANKET ION MILLING ON THE PROPERTIES OF SUPERCONDUCTING YBCO FILMS

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ABSTRACT

The effects of low-energy blanket ion milling on the electrical and structural properties of superconducting yttrium-barium-copper-oxide ($YBa_2Cu_3O_{7-x}$, or YBCO) were investigated. This process has proven not to have a detrimental effect on the electrical or structural properties of high-quality YBCO films. In fact, it has been found that, in many cases, the critical current density (J_c) improves as a result of a brief exposure to a low-energy ion beam. Also, milling of high-quality films results in a reduction in RMS surface roughness. Lower-quality films are typically degraded by the same process.

INTRODUCTION

The High-Density Electronics Center (HiDEC) at the University of Arkansas is conducting research directed at the fabrication of superconducting multi-chip modules (MCMs). These modules will consist of semiconducting ICs on a superconducting interconnect structure. The superconductor material of choice is YBCO. Due to the reactivity of YBCO with air and water, its surface develops a non-superconducting layer through processing and handling. It is desired that this layer be removed prior to metallization (preferably in-situ) to produce a low-resistance contact. Ion milling is under consideration to serve this purpose. Consequently, the effects of ion bombardment on the electrical and structural properties of YBCO must be investigated to determine the effectiveness of this process.

The proposed superconducting MCM interconnect structure consists of two superconducting planes separated by dielectric layers which are deposited on a substrate. This two-layer structure is based on the interconnected mesh power system (IMPS) MCM topology [1], in which the power, ground, and signal components are combined into two planes. Due to the high dependence on the crystallographic properties when interfacing ceramic materials, minimization of layers is critical in this structure.

The four-sided problem of lattice matching, coefficient of thermal expansion (CTE), interdiffusion, and dielectric constant prevent the use of a single material for the

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dielectric layer in this structure. The currently proposed dielectric layer for the HiDEC superconducting MCM consists of silicon oxide (Si_xO_y) buffered by layers of cerium dioxide (CeO_2) grown either by an ion beam–assisted sputtering or laser ablation technique. Si_xO_y has been chosen due to its low dielectric constant, and its extensive application in electronics. The Si_xO_y will be tailored by sputter deposition for the best trade-off between its dielectric constant and CTE. CeO_2 has been chosen to buffer between Si_xO_y and YBCO because of its lattice parameter and CTE match with YBCO.

The superconductor planes are to be connected by metal vias. Previous publications have illustrated the severe degradation of the critical current density (J_c) of a superconducting YBCO via [2]. This reduction in J_c is due to the anisotropic nature of current flow in YBCO [3]. In order to keep the YBCO layers planar, the Si_xO_y will be planarized prior to the second YBCO deposition, and the YBCO layers will be connected by reach-through vias. The ideal metal for low-resistance contact to YBCO is gold (Au). Other options are silver (Ag), platinum (Pt), or a multi-layer metal. A cross-sectional representation of the superconducting MCM interconnect structure is shown in Figure 1.

An item of extreme importance, not considered in the previous section, is that of the reactivity of YBCO with its surroundings. YBCO has been shown to be reactive with many of its environmental components, especially air and water [4-6]. This results in the formation of a non-superconducting surface layer on YBCO films upon exposure to air and conventional wet processing steps, such as photolithography. This reacted layer results in higher-resistance contacts and defeats the purpose of lattice matching at the interface of a dielectric and a reacted YBCO surface. Avoidance of these reactions by shielding YBCO from a reactive atmosphere would be very time consuming as well as expensive. Figure 2 shows the interconnect structure of Figure 1 taking into account a non-superconducting surface on the YBCO planes of the superconducting MCM interconnect structure.

EXPERIMENTAL PROCEDURES

Removal of the non-superconducting surface of YBCO is the most feasible solution to the reactivity problem. It is desirable for this removal process to be performed in the same chamber as the subsequent deposition step, so that the superconducting surface of the YBCO is not exposed to air. In the fabrication of the HiDEC module, where the CeO_2 layers are deposited by ion-beam assisted sputtering in the same chamber in which metallization is performed, the ion source may be used to etch the YBCO films until the superconducting bulk is exposed. This arrangement then allows for the deposition of the dielectric layer or metal following the in-situ milling process.

The use of inert ions to bombard a surface in order to remove material is called ion milling. Ion milling has been applied extensively to the patterning of YBCO films [7,8]. However, it has also been reported that it degrades the electrical properties of YBCO [9]. Since the surface preparatory process exposes the entire surface of the film

(this is where the term "blanket" comes from), a major concern is damage to the remaining film. In order to minimize the damage to the underlying superconducting YBCO, caused by exposure to ion milling, the process is performed at an energy lower than that common to bulk etching processes.

In order to evaluate the effects of low-energy blanket ion milling on YBCO films, the electrical properties of critical current density (J_c) and critical temperature (T_c) were measured prior to processing and after repeated exposures. The effects on the structural properties of YBCO were determined using atomic force microscopy (AFM) by which the surface structure was observed for changes and the surface roughness was calculated for a 100 μm^2 area.

Each milling step was performed at a beam energy of 500 eV and a beam current density of 0.3 mA/cm^2 for 2-minute intervals. The ion source was oriented normal to the sample surface at a distance of 15 cm. Argon gas was used to create the inert ions. The background pressure during milling was $1x10^{-4}$ Torr. Typically, bulk etching is performed at energies greater than 1000 eV and a current density of approximately 1 mA/cm^2. In order to minimize residual damage from ion bombardment, an energy of 500 eV and a current density of 0.3 mA/cm^2 was chosen for the work described here. The etch rate of YBCO for these etching parameters is approximately 100 Å/min, so about 200 Å were removed per exposure. The initial thickness of the films was approximately 3000 Å-4000 Å.

YBCO films were deposited by sputtering or laser ablation on yttria-stabilized zirconia (YSZ), lanthanum aluminate ($LaAlO_3$, or LAO), or strontium titanate ($SrTiO_3$, or STO) substrates. Measurements of J_c and T_c were performed using a non-contact system that employs a current induction technique [10]. AFM data was obtained with a Digital Instruments Dimension 3000 Scanning Probe Microscope. The ion milling was performed with an Ion Tech model FC3000 filament-type 3 cm ion source.

EXPERIMENTAL RESULTS

As previously noted, the intent of the surface preparation process is to remove the non-superconducting surface from YBCO without degrading its electrical or structural properties. However, what has been discovered is an improvement of J_c in some cases and typically a degradation of T_c. Figure 3 shows the plot of T_c for a YBCO film deposited by laser ablation onto a LAO substrate. As can be seen, the onset temperature remains the same while the zero temperature has degraded from 88 K to 83 K after one exposure to the blanket ion milling. Figure 4 shows a plot of critical current (I_c) for the same sample. For a crossover criterion of 20 V, I_c has increased from 11 mA to 25 mA, which corresponds to a J_c increase from $3.77x10^5$ A/cm^2 to $8.57x10^5$ A/cm^2.

Figures 5 and 6 show the T_c and I_c, respectively, of a YBCO film deposited by sputtering onto a YSZ substrate. After one exposure to blanket ion milling, T_c remained

unchanged at 88 K while I_c increased from 30 mA to 36 mA, which corresponds to a J_c increase from 1.029×10^6 A/cm^2 to 1.234×10^6 A/cm^2. Figures 7 and 8 show the T_c and I_c, respectively, of another YBCO film deposited by-sputtering on YSZ. After milling, the T_c remained unchanged at 87 K while the I_c increased from 32 mA to 52 mA, which corresponds to a J_c increase from 1.097×10^6 A/cm^2 to 1.783×10^6 A/cm^2.

Not all samples exposed to blanket ion milling behaved in this manner. Figure 9 plots the variation in I_c after each blanket mill for six samples. After one exposure to blanket ion milling, three of the films showed an increase in J_c, two showed a decrease, while one remained unchanged. After the second exposure, one film showed an increase in J_c, three showed a decrease, while one remained unchanged. One sample was milled three times and showed a continous decrease in J_c.

In addition to the electrical properties of YBCO, it is desirable that the surface roughness of the films not be degraded by the in-situ processing to promote epitaxy and planarity. Figure 10 plots the variation in RMS surface roughness (R_q) after each blanket mill for six samples. After one exposure to the blanket ion milling, three of the films showed a decrease in R_q, while three showed an increase. The films consistently showed an increase in R_q after subsequent exposures.

CONCLUSIONS

As discussed previously, the intent of the in-situ surface conditioning process described in this paper is to remove a non-superconducting surface without degrading the electrical or structural properties of YBCO. It has been shown that, in many cases, the J_c of YBCO films can be increased by a 2-minute exposure to an argon ion beam at 500 eV and 0.3 mA/cm^2. The increase in J_c is believed to be due to damage caused by the argon ions which creates flux pinning centers on the surface of the YBCO [11,12].

The effect on surface roughness of low-energy blanket ion milling are intriguing. While the films studied here showed some increase in surface roughness, the amount of the increase is acceptable considering that these films initially are sufficiently smooth for patterning of lines as small as 5 μm. It has also been found that films with poor initial roughness (>30 nm RMS) are consistently smoothed by low-energy blanket ion milling. The films that did show an increase in roughness initially contained many pits on the surface which were progressively worsened by the milling. Films which were initially pit-free were shown to decrease in roughness after milling, even for films which were initially very smooth (<10 nm RMS).

The effects of ion milling on the electrical properties of YBCO films correlate well with changes in roughness. Films which exhibited high quality initially were more likely to be improved by low-energy blanket ion milling. On the other hand, poorer quality films typically degraded with ion milling. However, the results of these experiments show that YBCO films can be exposed to low-energy blanket ion milling

with relatively little detrimental effect on their electrical or structural properties. In fact, it may be reasonable to perform ion milling with the intent of increasing the J_c of YBCO films.

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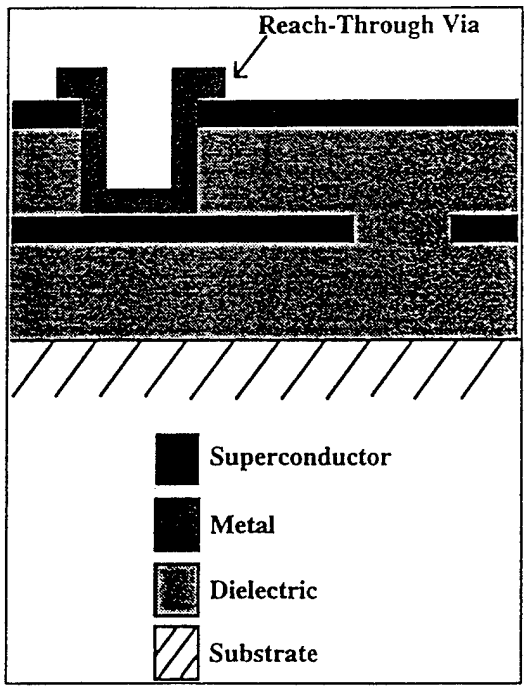

Figure 1: Interconnect Structure

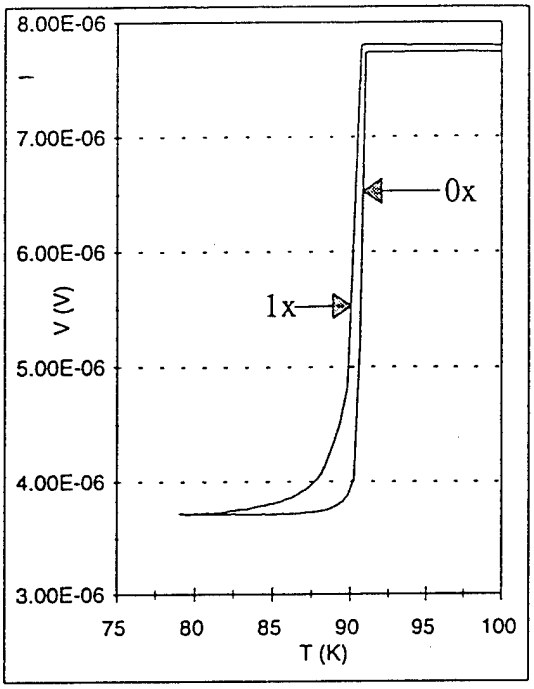

Figure 3: T_c of laser-deposited YBCO on LAO

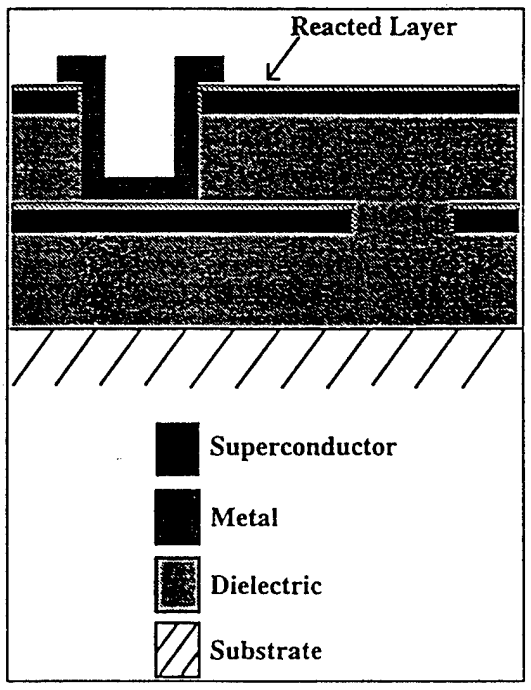

Figure 2: Reactivity of YBCO

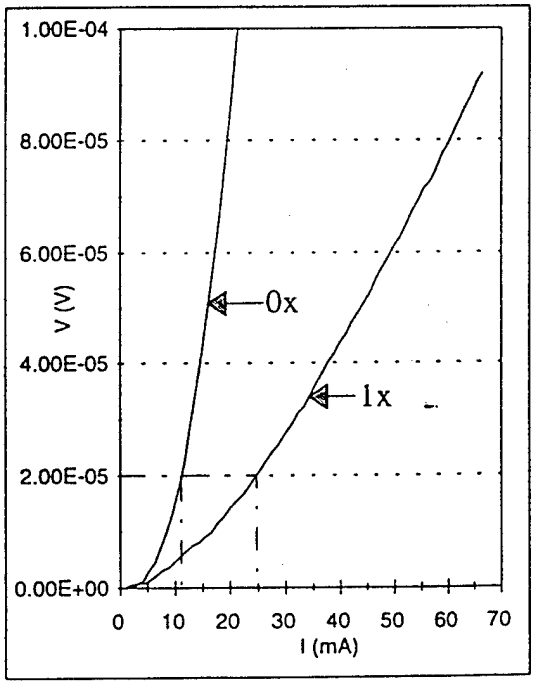

Figure 4: I_c of laser-deposited YBCO on LAO

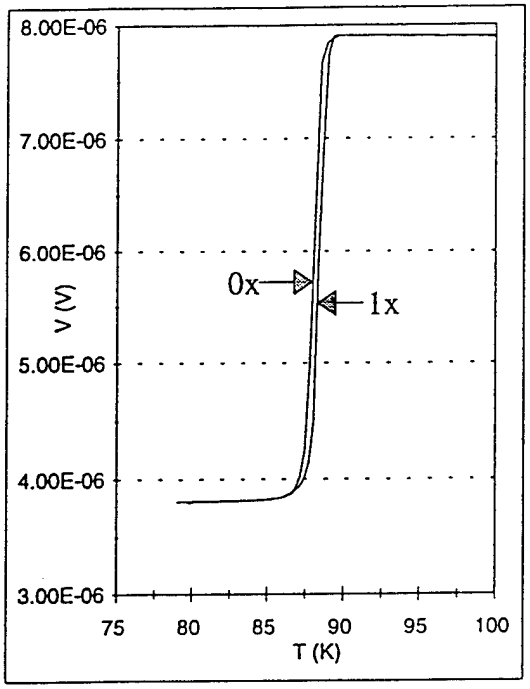

Figure 5: T_c of sputtered YBCO on YSZ

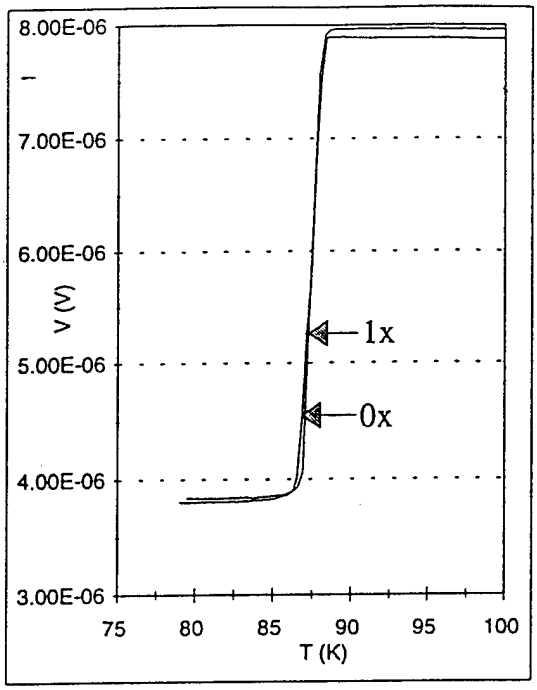

Figure 7: T_c of sputtered YBCO on YSZ

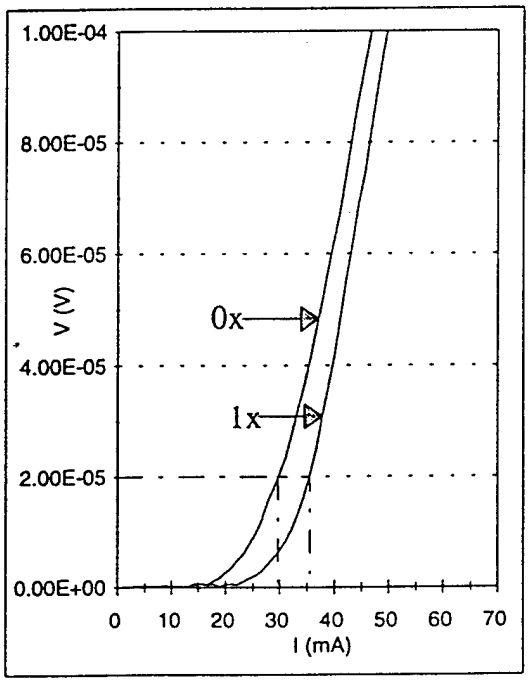

Figure 6: I_c of sputtered YBCO on YSZ

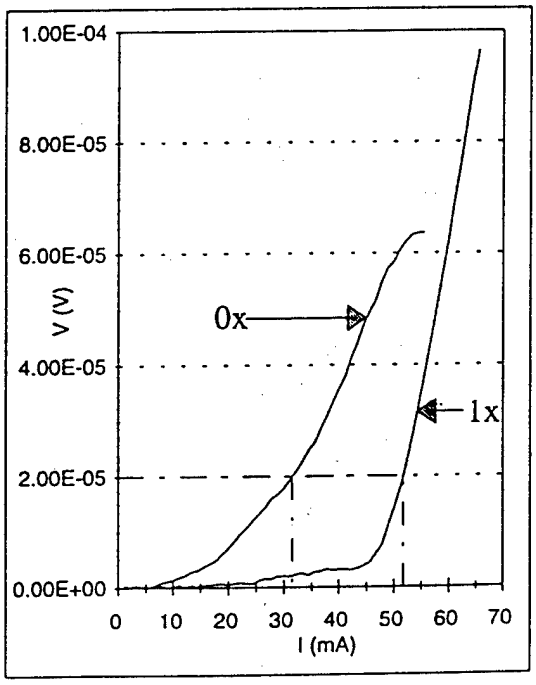

Figure 8: I_c of sputtered YBCO on YSZ

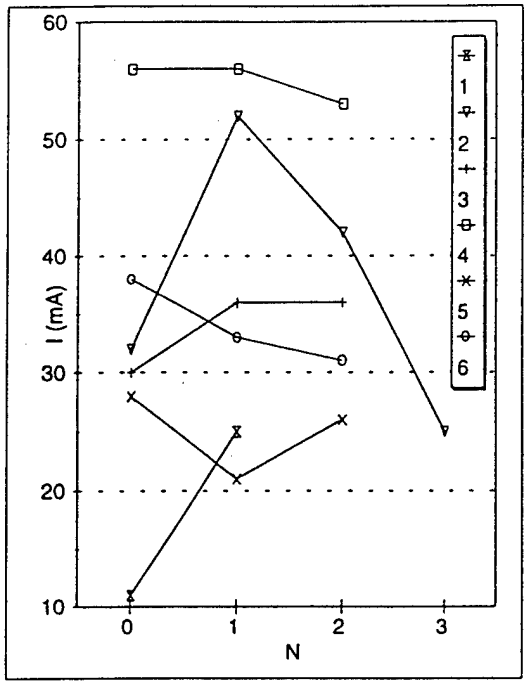

Figure 9: I_C vs. number of mills

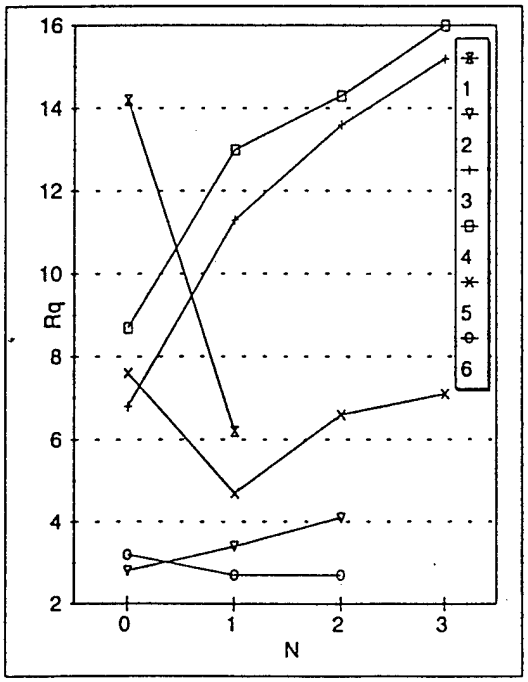

Figure 10: RMS roughness vs. number of mills

PROCEEDINGS OF THE SYMPOSIUM ON

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Magnetic field and temperature dependence of critical current densities in multilayer $YBa_2Cu_3O_{7-\delta}$ films

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In order to build high-temperature superconductor (HTS) multichip modules (MCMs), it is necessary to grow several epitaxial layers of YBCO that are separated by thick dielectric layers without seriously affecting the quality of the YBCO layers. In this work, we have successfully fabricated YBCO/YSZ/SiO_2/YSZ/YBCO structures on single-crystal $LaAlO_3$ substrates using a combination of pulsed laser deposition for the YBCO layers and ion-beam-assisted rf sputtering to obtain biaxially aligned YSZ intermediate layers. The bottom YBCO layer had a $T_c \sim 89$ K, $J_c \sim 7.2\times 10^5$ A/cm^2 at 77 K, whereas the top YBCO layer had a $T_c \sim 86$ K, $J_c \sim 6\times 10^5$ A/cm^2 at 77 K. The magnetic field and temperature dependence of J_c for the YBCO films in the multilayer have been obtained. The results for each of the YBCO layers within the YBCO/YSZ/SiO_2/YSZ/YBCO structure are quite similar to those for a good quality single-layer YBCO film. © *1996 American Institute of Physics.* [S0021-8979(96)03308-9]

I. INTRODUCTION

In electronic applications of high-temperature superconductor (HTS) thin films, the critical current density (J_c) is an important characteristic. One of the potential applications of high-temperature superconducting films is as electronic interconnects on a multichip module (MCM).[1] Since there are a minimum of two HTS thin films, separated by thick dielectric layers required, in HTS multichip modules (MCMs), it is necessary to know if the quality of the HTS layers is still maintained after the entire fabrication process is completed. In addition to the critical temperature (T_c) and critical current density at zero field, the dependence of J_c on an externally applied magnetic field and the temperature for the entire multilayer structure is crucial information for electronic applications. The YBCO/YSZ/SiO_2/YSZ/YBCO multilayer structure has been fabricated by Reade *et al.*[2] They reported cracking in the top YBCO layer, which limited their investigation of the properties of the multilayered structure.

In this article, we report a study of the temperature and magnetic field dependence of J_c for both YBCO layers in a YBCO/YSZ/SiO_2/YSZ/YBCO multilayer structure[3] performed by the magnetization method. Our results show that the temperature and magnetic field dependence of J_c of the YBCO layers of these samples are similar to those of high quality single-layer YBCO thin films.

II. EXPERIMENT

The YBCO/YSZ/SiO_2/YSZ/YBCO multilayer samples investigated here were prepared by using a combination of pulsed laser deposition and ion-beam-assisted magnetron sputtering. Details of the technique will be described elsewhere.[3] In short, a 200-nm-thick $YBa_2Cu_3O_{7-\delta}$ (bottom YBCO, layer 1) film was deposited on a single-crystal $LaAlO_3$ substrate (100 orientation and area 1×1 cm^2) by pulsed laser ablation at a substrate temperature of ~750 °C. Ion-beam-assisted rf sputtering was used to deposit biaxially aligned 200-nm-thick yttria-stabilized zirconia (YSZ) as a capping layer (layer 2). Next a 1-μm-thick, amorphous SiO_2 layer (layer 3) was deposited on layer 2 at room temperature by rf sputtering. The capping layer (YSZ) is used to prevent diffusion of the third SiO_2 layer into the top YBCO layer. A fourth layer (biaxially aligned YSZ) was then deposited on the SiO_2 layer to a thickness of 200 nm using the same method as for layer 2. This layer is very important. It not only functions as protection against the diffusion of the third SiO_2 layer into the YBCO layer, it also allows good epitaxial YBCO growth if it has a well-aligned structure. Finally, the top YBCO layer (layer 5) was deposited by laser ablation under the same conditions as was used for layer 1.

The orientation of the YSZ and YBCO layers was characterized by x-ray diffraction. The magnetization $M(H)$ loop was measured using a Quantum Design Magnetometer in fields up to 4 T, applied parallel to the c-axis direction and at a fixed temperature. This was repeated for different temperatures ranging from 5 to 77 K. The values of J_c were calculated using Bean's model. The electrical resistance was measured using the standard four-lead technique.

III. RESULTS AND DISCUSSION

X-ray diffraction data showed that all samples investigated here were single-phase highly c-axis oriented with very good in-plane epitaxy (Fig. 1). There were no cracks observed in the top YBCO layer. The resistance $R(T)$ and magnetization $M(T)$ of the samples were carefully measured for each YBCO layer. Figure 2 shows the typical resistance as a function of temperature for the top YBCO layer. The

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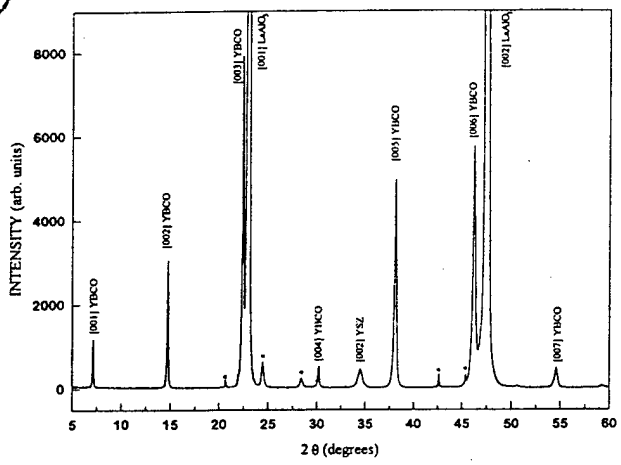

FIG. 1. θ-2θ x-ray diffractometer pattern for the YBCO/YSZ/SiO_2/ YSZ/ YBCO structure on [001] $LaAlO_3$ (*: indicate substrate impurity peaks seen in the bare substrates of the same batch).

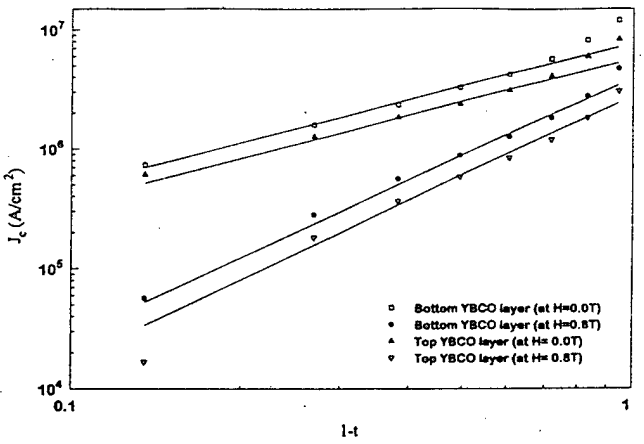

FIG. 3. Logarithmic plots of J_c vs $1-t$ for each of the YBCO layers within the multilayer structure. Straight lines are the curve fits to $(1-t)^n$, where $n\sim 1.3$ for $H=0.0$ T and $n\sim 2.1$ for $H=0.8$ T.

zero resistance temperature for this YBCO layer is about 86 K with a transition width of about 2 K. The $M(T)$ data for a multilayer sample are shown in the inset of Fig. 2. As can be seen in the inset of Fig. 2, the onset transition of the $M(T)$ curve is about 89 K. A second transition (indicated by the arrow in the inset of Fig. 2) is consistent with the T_c of the top YBCO layer measured by the transport method (Fig. 2). In order to verify this, T_c was remeasured again after the top layer of YBCO was etched away by using a dilute EDTA solution, and the onset transition was found to be about 89 K.

The critical current density J_c of the samples were measured by the magnetization method and calculated using Bean's model. For a rectangular single-layer film, J_c can be calculated from the following formula:[4]

$$J_c = 10[M_+(H) - M_-(H)]/L_1[1-(L_1/3L_2)]V. \qquad (1)$$

In Eq. (1), $M_+(H)$ and $M_-(H)$ are the magnetization of the decreasing and increasing field branches in electromagnetic units (emu), respectively; V is the volume of the thin film in cm^3; L_1 and L_2 are the short and long sides of the samples in cm, respectively. We have assumed that J_c is independent of the B field and excluded the anisotropic critical currents in the above calculation. In order to determine J_c of both the top and bottom YBCO layers, the magnetization $M^m_+(H)$ and $M^m_-(H)$ for the multilayer film was measured first, then the magnetization $M^b_+(H)$ and $M^b_-(H)$ for the bottom layer was measured after the top layer of YBCO was etched away. In this article we use superscript t and b for the parameters related to the top and bottom YBCO layer in the multilayer film, then J_c for the bottom layer should be

$$J^b_c = 10[M^b_+(H) - M^b_-(H)]/L^b_1[1-(L^b_1/3L^b_2)]V^b, \qquad (2)$$

and for the top layer in the multilayer film,

$$J^t_c = 10\{[M^m_+(H) - M^b_+(H)] - [M^m_-(H) - M^b_-(H)]\}/L^t_1[1-(L^t_1/3L^t_2)]V^t. \qquad (3)$$

The J_c of the top YBCO layer was found to be about 6×10^5 A/cm^2, and a value of $\sim 7.2\times 10^5$ A/cm^2 was obtained for the bottom layer at 77 K under zero magnetic field. J_c, as a

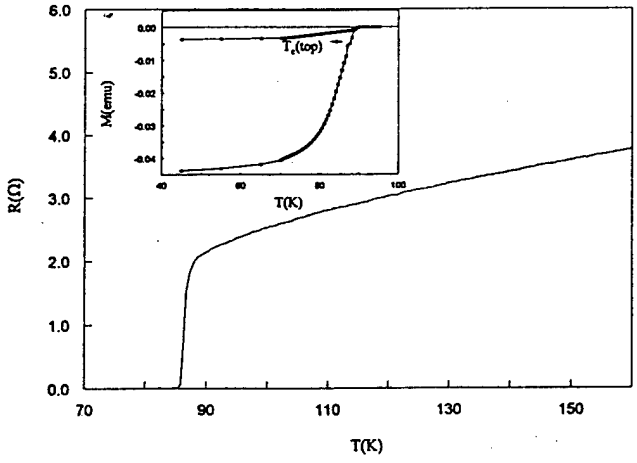

FIG. 2. Resistance vs temperature for the top YBCO layer in the YBCO/YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ multilayer structure. Inset: magnetization M as a function of T for the entire multilayer structure.

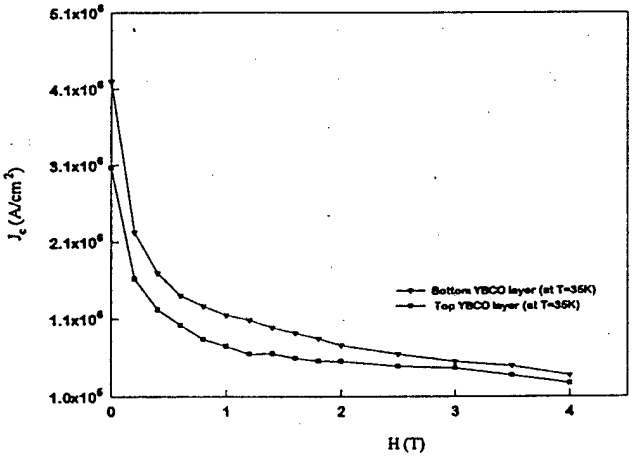

FIG. 4. Magnetic field dependence of J_c for top and bottom YBCO layers at 35 K. Field is applied perpendicular to $a-b$ plane.

function of $(1-t)$, is shown in Fig. 3 for different values of the magnetic field, where $t=T/T_c$. It was found that, for both YBCO layers, the temperature dependence of J_c is similar to that for a good quality, single-layer YBCO film.[5–7] The magnetic field dependence of J_c for both YBCO layers at 35 K are shown in Fig. 4. It clearly shows that J_c for both top and bottom YBCO films essentially has the same magnetic field dependence as that for the high quality, single-layer YBCO film.[5–7]

IV. SUMMARY

A good quality YBCO multilayer structure has been fabricated using laser ablation and ion-beam-assisted rf sputtering. The dependence of J_c on the temperature and magnetic field for both YBCO layers in the multilayer has been determined. The results suggest that the temperature and magnetic field dependence of J_c of the YBCO layers in the multilayer structure are not altered appreciably by the multilayer growth processes.

ACKNOWLEDGMENTS

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POSTER

HQ-15

THE MAGNETIC FEILD AND TEMPERATURE DEPENDENCE OF CRITICAL CURRENT DENSITIES IN MULTILAYER $Y_1Ba_2Cu_3O_{7-\delta}$ FILMS

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In order to build high temperature superconductor (HTSC) multichip modules(MCM's), it is necessary to grow several epitaxial layers of YBCO that are separated by dielectric layers without seriously effecting the quality of the YBCO layers. In this work, we have successfully fabricated YBCO/YSZ/SiO_2/YSZ/YBCO on single crystal $LaAlO_3$ substrates using a combination of pulsed laser deposition for the YBCO layers and ion beam assisted sputtering to obtain biaxially aligned YSZ intermediate layers. The bottom YBCO layer had a T_c~89K, J_c 10^6 A/cm^2 at 77K, whereas the top YBCO layer had a T_c~86K, J_c 10^6 A/cm^2 at 77K. The magnetic field and temperature dependence of J_c in these multilayer YBCO films has been obtained. The results from YBCO/YSZ/SiO_2/YSZ/YBCO and YBCO/YSZ/SiO_2/YSZ are quite similar to that from a single layer YBCO film.

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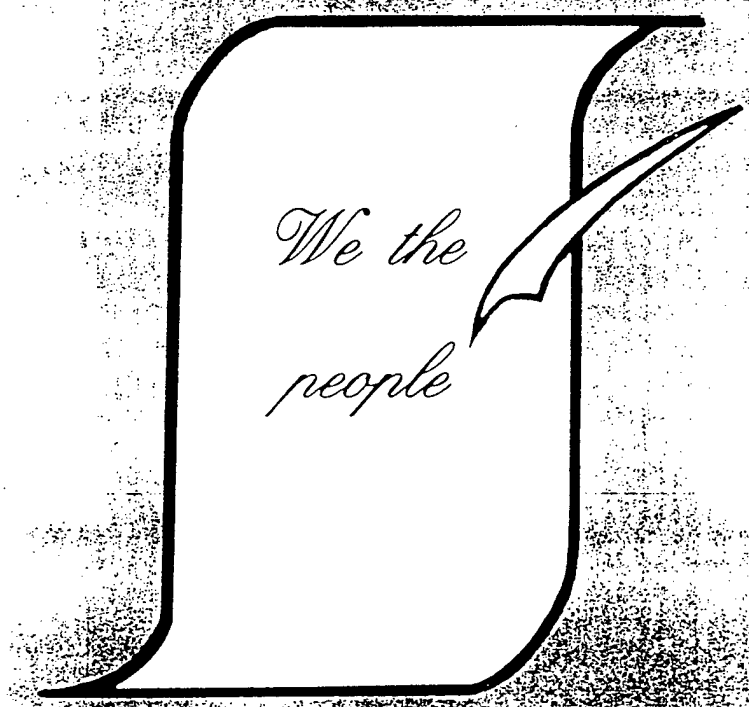
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PRESENTATION: Paper

FABRICATION OF HIGHLY TEXTURED SUPERCONDUCTING THIN FILMS ON POLYCRYSTALLINE SUBSTRATES USING ION BEAM ASSISTED DEPOSITION

[1]Q. Xiong, [1]S. Afonso, [1]F.T. Chan, [1]K.Y. Chen, [1]G.J. Salamo, [2]G.Florence, J. Cooksey, S. Scott, [2]S. Ang, [2]W.D. Brown and [2]L. Schaper,
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ABSTRACT

$Tl_2Ba_2CaCu_2O_y$(Tl2212) thin films on ceramic Al_2O_3 substrates with J_c(77K) of about 10^5 A/cm^2 and high quality YBCO/YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ mutilayers with J_c(77K) of about 6×10^5 A/cm^2 in the top YBCO layer have been successful deposited for the first time. These Mirror-like, highly c-axis oriented films were grown on highly textured YSZ buffer layers, which were deposited through Ion Beam-Assisted Laser Ablation. The zero resistance temperature is 95-108K for the Tl2212 films, and 85-90K for the multilayer YBCO films. The results suggest that using cheap non-single crystal substrates to fabricate good HTS films is possible.

I. Introduction

Since the discovery of high temperature superconductors(HTS), many possible applications of HTS thin films have been design and demonstrated, from very useful fault current limiters to the electronic interconnects on multichip module (MCM) substrates. All of these applications would benefit from the use of HTS thin films. One of the major problems for the application of HTS's is that HTS's can carry only a limited amount of current without resistance. This problem is related to their two dimensional layered structure. According to earlier studies[1-2], if the layers do not line up properly, the critical current density will decrease dramatically in the misaligned region. One way to overcome this problem is to grow micron-thin layers of the material on well organized substrates, epitaxally. The process has the effect of lining up the superconducting layers more accurately. HTS thin films grown on single crystal substrates of $LaAlO_3$ or $SrTiO_3$ have good lattice match between the HTS and substrate, and have critical current densities of about ~10^6 A/cm^2, which is large enough for most HTS thin film applications. While this effort is impressive, it is far from useful, since the films so developed are much too expensive because the single crystal substrates are very expensive and available only in relatively small sizes. Moreover, for some electronic applications such as HTS multi-chip modules(MCM's),

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there are at least two HTS thin films that are separated by thick dielectric layers. Useful dielectric layers such as SiO_2 have noncrystalline structures. For this reason, HTS thin film layers cannot be grown on the dielectric layer with good alignment by conventional methods. Recent studies[3-7] have shown that highly biaxially aligned YSZ layers can be grown on non-crystalline substrates, which are cheaper and easy to get in any size needed by Ion beam-assisted laser deposition(IBAD). Using this method, high quality $YBa_2Cu_3O_y$ (YBCO) films have been deposited on biaxially aligned YSZ layers grown on non-crystalline substrates with J_c's of up to 8×10^5A/cm^2 at 75K.

Here, we report the results from Tl2212 films fabricated on polycrystalline Al_2O_3 substrates with an IBAD deposited YSZ buffer layer and YBCO/YSZ/SiO_2/YSZ/YBCO/$LaAlO_3$ mutilayers.

II Experimental

Fine polished Al_2O_3 was used for the substrates of the Tl2212 films. Ion-beam assisted pulsed laser deposition was used to prepare highly biaxial aligned YSZ buffer layers at room temperature. While YSZ was deposited by pulse laser deposition, an Ion-beam (argon ion source) bombarded the substrates at an angle of 55° from the substrate normal. The laser used here was an ArF excimer laser (wavelength = 193 nm, shot frequency = 5 Hz). The energy density of the laser beam, which was focused on the YSZ target, was set to about 2 - 3 J/cm^2. The ion beam energy was typically set at about 250 eV, and the beam current density was about 120 μA/cm^2. The oxygen partial pressure was maintained at 3×10^{-4} Torr, and with the ion beam the total pressure in the vacuum chamber was about 8×10^{-4} Torr during the deposition of the YSZ layers. The substrate temperature increased to about 100 °C due to the assisting ion beam. The growth rate was about 0.5 Å/S. The thickness of the YSZ buffer layers in our experiment was about 5000 Å. For the YBCO multilayer structure, 2000 Å thick YBCO layers were deposited by pulsed laser ablation at ~ 750 °C. A 4-5 micron thick amorphous SiO_2 layer was deposited as a dielectric layer at room temperature by rf sputtering. For the Tl2212 films, 2000~3000Å $Ba_2CaCu_2O_y$ precursor films were deposited on the YSZ-buffer layer at a temperature of 400°C using pulsed laser ablation. The films were then treated in a thallination process at 810°C.

The structures of deposited films were characterized by x-ray diffraction. T_c and J_c of HTS layers were measured by both transport method using the standard four-lead technique and the magnetization method using a Quantum Design Magnetometer.

III. Results and Discussion

All YSZ films deposited on the polycrystalline Al_2O_3 substrates for Tl2212 or on first YBCO layer, or on amorphous SiO_2 layer were (001) oriented with the <001> axis normal to the substrate plane. A typical X-ray θ-2θ diffraction pattern for a YSZ film deposited on a polycrystalline Al_2O_3 substrate is shown in Fig.1. Observation of only the YSZ(002) peak in the

X-ray θ-2θ diffraction pattern indicates that the YSZ was highly (001) oriented. The ϕ scan width of the {111} peaks is about 25° (FWHM).

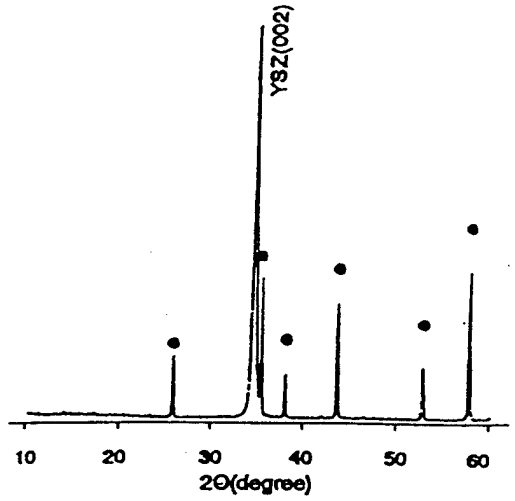

Fig. 1. X-ray diffraction θ-2θ scan of YSZ on Al_2O_3 (● Al_2O_3 peak)

Typical resistance versus temperature data for Tl2212 is shown in Fig.2. The zero resistance temperature T_c is 105.6K which is comparable with the results from the high quality films grown on $LaAlO_3$ or $SrTiO_3$ substrates. The critical current densities of these films are about 8×10^4 A/cm^2 by transport method. Fig.3 shows the typical resistance as a function of temperature for the top YBCO layer in the multilayer structures. The zero resistance temperature for this YBCO layer is about 86K with a transition width of about 2 K. The Messier effect M(T) for the same mutilayer sample is shown in the inset of Fig.3. As in the inset of Fig.3, the onset transition of the M(T) curve is at about 89 K, a second transition (indicated by the arrow) in the inset of Fig.3 is consistent with the T_c of the top YBCO layer measured by the transport method (Fig 3). In order to verify this, T_c was remeasured again after the top layer of YBCO was etched

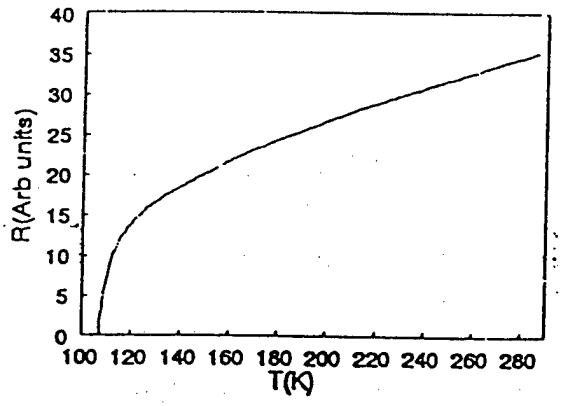

Fig. 2. Resistance vs. Temperature for the $Tl_2Ba_2CaCu_2O_8$ on YSZ/Al_2O_3.

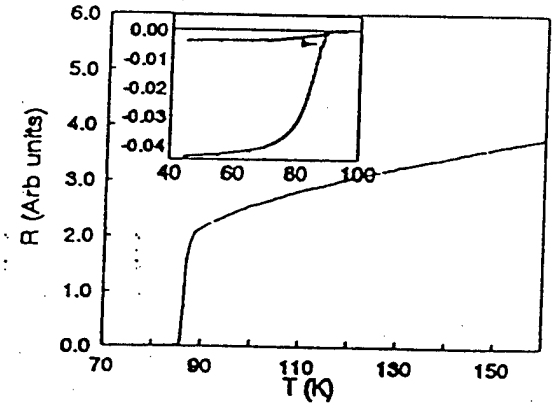

Fig. 3. Resistance vs temperature for the top YBCO layer in the YBCO/YSZ/SiO_2/YSZ/YBCO/ $LaAlO_3$ multilayer. Inset: Magnetization M as a function of temperature for the entire multilayer.

away by using a dilute EDTA solution, and the onset transition was found to be at about 89 K without the second transition. The critical current density, J_c of the samples were measured by the

magnetization method and calculated using Bean's model before and after the top layer of YBCO was etched away. The J_c of the bottom YBCO layer is about 7.2×10^5 A/cm^2 at 77 K, and of the top YBCO layer is about 6×10^5 A/cm^2 at 77 K, For comparison, we deposited both YBCO and Tl2212 on ceramic Al_2O_3 substrates. Even though the T_c of these films were about the same, J_c is $< 10^4$ A/cm^2. Which is about two orders of magnitude lower than that of the film on the biaxially aligned YSZ layer

IV. SUMMARY

Tl2212 films on ceramic Al_2O_3 substrates have been grown for the first time and good quality YBCO multilayer structures have been prepared using laser ablation and ion beam assisted rf sputtering. Our results demonstrate that good quality HTS films can be grown on cheap nonsingle crystal substrates though the Ion Beam-assisted deposition technique.

ACKNOWLEDGMENTS

This work is supported in part by NSF DMR 9318946, DARPA (Contract No. MDA 972-90-J-1001) through Texas Center for Superconductivity at the University of Houston.

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PROCEEDINGS of the 10th ANNIVERSARY HTS WORKSHOP

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Fabrication and characterization of vias for contacting $YBa_2Cu_3O_{7-x}$ multilayers

J. W. Cooksey, S. Afonso, W. D. Brown, L. W. Schaper, S. S. Ang, R. K. Ulrich, G. J. Salamo, and F. T. Chan

High Density Electronics Center, University of Arkansas, 600 W. 20th Street, Fayetteville, AR 72701 USA

In order to connect multiple layers of high temperature superconductor (HTS) interconnects, low contact resistance vias must be used to maintain high signal propagation speeds and to minimize signal losses. In this work, 40 μm via contacts through $YBa_2Cu_3O_{7-x}$ /$SrTiO_3$/SiO_2/YSZ/$YBa_2Cu_3O_{7-x}$ multilayers utilizing dry etching techniques and sputter deposited Au for contacting through the vias have been successfully fabricated and characterized. The vias connect two laser ablated $YBa_2Cu_3O_{7-x}$ (YBCO) signal lines through thick (4-5 μm) SiO_2 insulating layers. This approach to making multilayer superconductor vias provides a low resistance contact between the YBCO layers while maintaining space efficiency and fabrication compatibility with the superconductor.

1. INTRODUCTION

Since the discovery of high temperature superconductivity (HTS), researchers have utilized their low resistance behavior in many applications. One such application is that of multichip modules (MCMs.) Unlike that of VLSI technologies where smaller feature sizes in successive generations allow interconnect lengths and power dissipation to be reduced, MCMs will not have that same luxury. As the complexity of ICs advances, pinout count per IC increases, and operating frequencies increase, MCM normal metal interconnections will have to grow in length and will not be allowed to reduce in cross-sectional area. On MCM-D substrates, typical copper or aluminum interconnection dimensions are about 2 to 5 μm in thickness and between 15 and 30 μm wide with corresponding via sizes. By cooling the metal to 77 K (liquid nitrogen temperature), the resistivity of copper decreases by a factor of about 7 which allows a corresponding decrease in the interconnect's cross-sectional area. In order to increase the wiring density beyond that of cryo-cooled MCMs and improve the chip-to-chip bottleneck at high frequencies, alternatives to conventional metal interconnects must be considered [1].

HTS interconnections, with negligible resistivity at operating frequencies of several tens of GHz and lower, have great potential to reduce an interconnect's cross-sectional area with typical thicknesses of less than 1 μm and widths of less than 2 μm for MCM applications with similar spacings. The main challenge for attaining multiple layers of high density, high performance HTS interconnects appears to be in fabricating compact, low resistance vias.

The work presented here focuses on this problem and describes a method of fabricating noble metal vias for use in an HTS MCM prototype.

2. EXPERIMENTAL DETAILS AND RESULTS

A cross-section of our multilayer YBCO structure utilizing Au vias is shown in Figure 1.

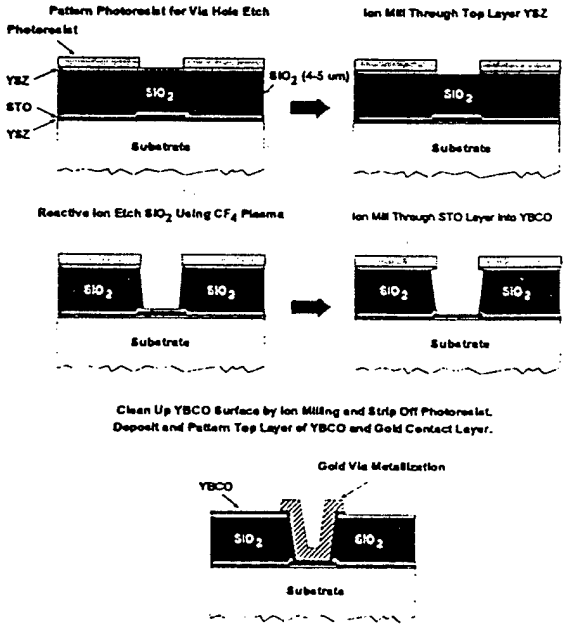

Figure 1. HTS via process.

Our research has centered around two layers of laser ablated $YBa_2Cu_3O_{7-x}$ (YBCO) interconnects separated by a multilayer dielectric consisting of $SrTiO_3/SiO_2/YSZ$. We are able to attain critical current densities > 5 x 10^5 A/cm^2 in both YBCO layers. The $SrTiO_3$ (STO) and YSZ (yttria-stabilized zirconia) layers being ~0.5 μm thick while the SiO_2 ranges between 4 and 5 μm.

The via fabrication process is as shown in Figure 1. The etching involves a 500 eV ion mill through the top YSZ buffer layer, which is followed by a reactive ion etch through the SiO_2 interlevel dielectric selectively stopping at the barrier layer of STO. To complete the etching process, a 500 eV ion mill is done to etch through the STO. The final milling is very nonselective and requires close observation to keep from overetching through the bottom layer of YBCO. When depositing the top layer of YBCO at ~700° C, whatever material is deposited on the via sidewalls is presumably corroded due to interdiffusion of Si from SiO_2 into the YBCO but, presumably, does not effect the quality of the via. The subsequent *in situ* deposition of ~2000 Å of Au by laser ablation creates low resistance contacts without having to do a high temperature anneal in oxygen as was described by Ekin et al. [2]. In similar structures, contact resistivities of less than 10^{-7} Ω-cm^2 have consistently been attained. An additional 1.5-2.0 μm of Au is deposited over the existing YBCO/Au and then patterned using ion milling and photoresist as a mask.

This type of via structure has several advantages over previously demonstrated superconducting vias for use in HTS MCMs [3,4]. Since HTS thin films need to be deposited on planar surfaces or gradual slopes to maintain a reasonable current density, due to grain boundary problems, they require gradually sloped via holes that take up a wide area. By using a noble metal, compact, high-aspect ratio vias can be fabricated reliably.

Ultrasonic Al wire bonds were then made between YBCO/Au bond pads on the substrate and a wire bondable PC board. Via chain resistance was measured using a conventional 4-point contact configuration and measuring the voltage drop across the vias while passing DC current through it. The resistance vs. temperature of a ~0.5 cm long via chain structure with ten 40 μm square vias interconnecting 50 μm wide YBCO lines is shown in Figure 2. The room temperature resistance was measured to be about 515 Ω, and upon cooling to 78.5 K, the resistance

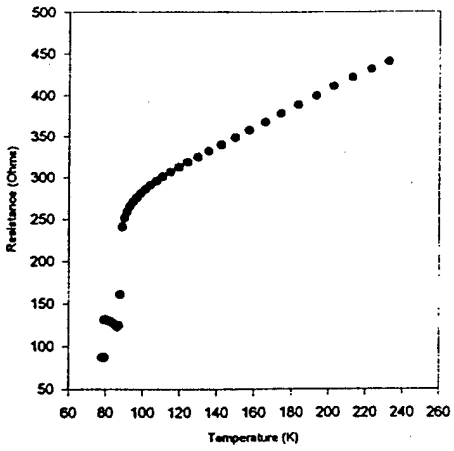

Figure 2. Temperature transition of a chain of ten 40 μm wide vias.

dropped to about 87 Ω. As is shown in Figure 2, there are two separate superconducting transitions occurring at about 89 K and 80 K which correspond to the top and bottom layer YBCO transitions. At 78.5 K, the interconnects had not yet become fully superconducting.

In summary, 40 μm YBCO/Au via chain structures have been characterized. The preliminary work shown here is to be improved upon by improving the quality of the YBCO layers, lowering the contact resistances, and possibly improving the step coverage of Au through the via by increasing its thickness.

ACKNOWLEDGEMENT

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5th International Conference on Materials and Mechanisms of Superconductivity, and High-Temperature Superconductors

February 28-March 4, 1997, Beijing, China

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Dear Dr. John W Cooksey,

We are pleased to inform you that your paper

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Title: Fabrication and Characterization of Vias for Contacting YBa2Cu3O7-x Multilayers
Co-Authors: S. Afonso W D Brown L W Schaper S S Ang R K Ulrich G J Salamo F T Chan

has been accepted for presentation at the M^2S-HTSC-V Conference. The instruction for preparing the manuscript will be sent to you directly by Physica C, Elsevier Science B.V.. The deadline for submitting the manuscripts is extended to **January 31, 1997,** but the earlier submission is preferable. Please mention the reference number in the further communication.

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Z. Z. Gan

Zhong-Xian ZHAO Zi-Zhao GAN Guo-Zhen YANG
Co-chairmen of M^2S-HTSC-V

PRESENTATION: Paper

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Fabrication techniques and electrical properties of $YBa_2Cu_3O_{7-x}$ multilayers with rf sputtered amorphous SiO_2 interlayers

[a]S. Afonso, [a]K. Y. Chen, [a]Q. Xiong, [a]F. T. Chan, [a]G. J. Salamo, [b]J. W. Cooksey, [b]S. Scott, [b]S. Ang, [b]W. D. Brown, and [b]L. W. Schaper.

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We have successfully fabricated $YBa_2Cu_3O_{7-x}$/YSZ/SiO_2/YSZ/$YBa_2Cu_3O_{7-x}$ multilayer structures on single crystal $LaAlO_3$ (100), substrates. The $YBa_2Cu_3O_{7-x}$(YBCO) layers were deposited using pulsed laser ablation (PLD), the biaxially aligned YSZ (250 nm thick) layers were deposited using ion beam assisted PLD (IBAD-PLD), and an amorphous SiO_2 (1-2μm) layer fabricated via rf sputtering was sandwiched between the YSZ layers. Fabrication techniques and characterization results are reported for patterned layers in this work.

1. INTRODUCTION

For high temperature superconductor multichip module(HTS-MCM) applications the basic building block is the HTS/Insulator (thickness >1μm)/HTS structure. A HTS-MCM can be defined as a miniaturized version of a multilayered printed wiring board with superconducting interconnects. Previously such a HTS-MCM prototype using a YBCO/$SrTiO_3$(500nm)/YBCO has been successfully fabricated by Burns et al [1]. Recently the use of ion beam assisted deposition to deposit biaxially aligned YSZ buffer layers on polycrystalline or amorphous substrates allowed for good quality YBCO films on these substrates [2-5]. Reade et al [6] were able to demonstrate using the ion beam assisted pulsed deposition (IBAD-PLD) technique that it was possible to fabricate the YBCO/YSZ-/amorphousYSZ(5μm)/YSZ/YBCO multilayers on oriented YSZ substrates with the top YBCO T_c ~ 87 K. They also fabricated the same structure using amorphous SiO_2, but cracks in the top YBCO layer did not permit electrical measurements of the top layer. The main advantage of SiO_2 is its low dielectric constant (~ 3.89), which makes it an ideal insulator material for MCMs.

In this paper we briefly describe the method to fabricate and the results obtained from the characterization of the YBCO/YSZ-/SiO_2/YSZ/YBCO multilayers.

2. EXPERIMENTS

The first YBCO layer (300nm thick) was fabricated by pulsed laser deposition using standard conditions. After patterning, part of the pads were masked to allow for transport measurements later. Next a 250 nm thick YSZ layer was deposited via IBAD PLD using conditions described in [5]. After this a 1-2 μm thick SiO_2 layer was deposited by reactively sputtering a Si target in oxygen ambient (the details of this process are described in [4]). Following the SiO_2 deposition another 250 nm thick biaxially aligned YSZ buffer/capping layer was deposited via IBAD PLD. Finally the masks were taken off and the top YBCO was deposited using the same conditions as the first YBCO except that the deposition temperature was kept ~ 20-30° lower. For the first set of multilayers the top YBCO layer was patterned into bridges over the underlying bridge patterns but shifted a little to the side so that the top bridge goes over step edges. The patterning was carried out by using photolithography and ion milling. For the second set of multilayers the top YBCO layer was patterned into

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bridges whereas the bottom YBCO layer was not patterned. Finally in the third set the top YBCO layer was patterned into serpentine (meander) lines crossing over the patterned bottom YBCO serpentine lines

3. RESULTS

The X-ray diffraction pattern for an unpatterned multilayer in Fig. 1. shows that the films have good *c*-axis orientation. We also measured the top YBCO ϕ scan full width at half maximum (FWHM) ~ 26° (for the (103) peaks), while for YSZ (111) peaks the FWHM was ~ 2-3° greater than that of the top YBCO.

For the first set, the bottom 40 μm wide bridge the T_c ~ 90 K and J_c ~ 2×10^6 A/cm² whereas for the top YBCO bridge 60 μm wide (with step edges), the T_c ~ 86-87 K and J_c ~ 3×10^4 A/cm². In the second set, the top YBCO bridge patterns of the same width without step edges the J_c ~ 10^5 A/cm² with Tc ~ 87-88 K. Finally in Fig. 2(A) is shown the resistance versus temperature plot for 20 μm serpentine bottom YBCO line 19 cm long the T_c ~87 K and J_c ~2×10^5 A/cm², whereas the same width serpentine line on the top layer showed semiconducting behavior as seen in Fig.2(B).

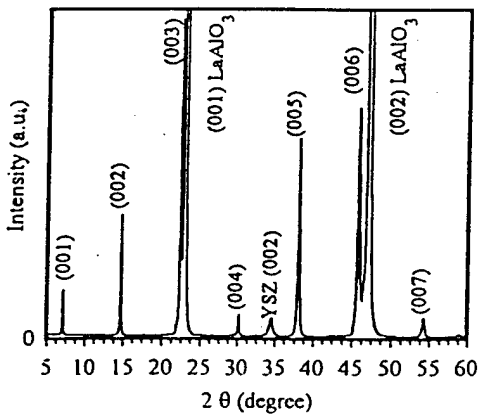

Fig. 1. X-ray diffraction pattern for a multilayer YBCO/YSZ/SiO_2/YSZ/YBCO sample

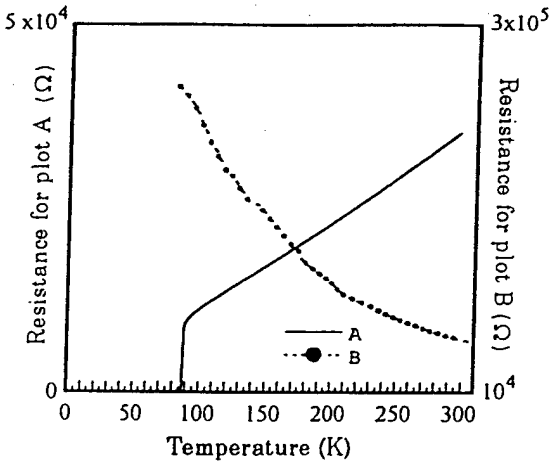

Fig. 2 Resistance versus temperature curves for (A) 20 μm wide bottom YBCO serpentine line, (B) 20 μm wide top YBCO serpentine line

4. CONCLUSIONS

Good quality YBCO layers separated by an amorphous SiO_2 interlayer have been fabricated by using biaxially aligned YSZ layers. However if the bottom YBCO is densely patterned then planarization is necessary to prevent degradation of superconducting properties at the step edges.

ACKNOWLEDGEMENT

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has been accepted for presentation at the M^2S-HTSC-V Conference. The instruction for preparing the manuscript will be sent to you directly by Physica C, Elsevier Science B.V.. The deadline for submitting the manuscripts is extended to **January 31, 1997,** but the earlier submission is preferable. Please mention the reference number in the further communication.

As the chairmen of the conference, we would like to invite you for an active participation in the M^2S-HTSC-V, which will be held in Beijing, Feb. 28-Mar. 4, 1997.

We will send you an official invitation letter for visa application after receiving your registration form, since your personal information (e.g. Passport Number etc.) is required in the letter. Please send us your registration form before **December 1, 1996.** If the registration form is not available, you may get it from the homepage of M^2S conference at **http://sun1.bham.ac.uk/hey/conferences/**, or directly ask us for it.

We are looking forward to meeting you at the M^2S-HTSC-V in Beijing.

Sincerely yours,

Z. Y. Gan

Zhong-Xian ZHAO Zi-Zhao GAN Guo-Zhen YANG
Co-chairmen of M^2S-HTSC-V

PRESENTATION: Paper

Recent Advances in High Temperature Superconductor Multichip Modules

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Abstract

Two different techniques for fabricating high temperature superconducting (HTS) MCM-D substrates have been developed and tested. The first unit consists of two digital gallium arsenide bare die connected by $YBa_2Cu_3O_{-\delta}$ (YBCO) HTS interconnects to form two ring oscillators on a 2.25 cm² MCM-D substrate. The interconnections consist of two wiring layers of YBCO separated by a 4-5 μm silicon dioxide interlevel dielectric. The signal lines are routed between power and ground lines which form an interconnected mesh power system (IMPS) and, thereby, the module avoids the necessity of having two additional layers for power and ground planes. Connection between the two YBCO layers is accomplished with low contact resistance 40 μm gold vias through the interlevel dielectric layer. The signal interconnects have 50 μm linewidths and 75 μm spacings. Electrical connections between the die and the MCM substrate and between the substrate and the PC board were made using ultrasonic Al wire bonds to low contact resistance gold/YBCO bond pads on the MCM substrate.

The second module, known as the Flip-Mesh superconducting MCM, provides an alternative to the multilayer MCM-D substrate described above. It involves using flip chip bonding techniques to connect multiple single-layer substrates, thereby reducing the processing complexity of fabricating multiple layers. X-plane and Y-plane interconnects are fabricated on separate substrates and interconnected using solder bumps. The IMPS topology is also utilized in this structure so that power, ground, and signals can be fabricated on two planes. The initial Flip-Mesh design incorporates 100 μm (4 mil) solder bump vias with similar spacings, which results in a low packing density for MCM-D technology, but a high density for I/O technology.

Key words: High temperature superconductors, MCM-D, Interconnected Mesh Power System (IMPS), YBCO

Introduction

Unlike that of VLSI technologies where smaller feature sizes in successive generations allow interconnect lengths and power dissipation to be reduced, multichip modules (MCMs) will not have that same luxury. As the complexity of ICs advances, pinout count per IC increases, and operating frequencies increase, MCM normal metal interconnections will have to grow in length and will not be allowed to reduce in cross-sectional area. On MCM-D substrates, typical copper or aluminum interconnection dimensions are about 2 to 5 μm in thickness and between 15 and 30 μm wide. The resistivity of copper or aluminum decreases by at least a factor of 7 when decreasing the temperature from 300 K to 77 K (liquid nitrogen temperature), which allows smaller cross-section interconnections to be fabricated on cryo-cooled MCMs. In order to increase the wiring density in MCMs beyond that of cryo-cooled MCMs and improve the chip-to-chip bottleneck at high frequencies, alternatives to conventional metal interconnects must be considered [1].

High temperature superconductor (HTS) interconnections, with negligible resistivity at operating frequencies of several tens of GHz and lower, have great potential to reduce the interconnection line cross-section even further with typical thicknesses being less than 1 μm and widths could be reduced to less than 2 μm for MCM applications. The critical current density of HTS interconnects, which limits the line's minimum cross-section, is similar in value to the maximum current density allowed in Al interconnects to inhibit electromigration. These small, low resistance

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interconnects offer significant performance advantages over normal metal interconnects for MCM-D technology using CMOS or GaAs integrated circuits which have enhanced chip level performance at liquid nitrogen temperatures (77 K). An added benefit of HTS lines is the reduced capacitive coupling between adjacent interconnections (due to their reduced thickness) which allows the lines to be spaced more closely together. The reduced cross-section of HTS interconnects should allow a significant increase in packing density and a corresponding decrease in the number of interconnect layers required to achieve the same functionality with normal metal interconnects.

We have been developing two separate HTS MCM prototypes. One is to be the first planar HTS MCM utilizing a thick layer of silicon dioxide as an interlevel dielectric and is based on MCM-D technology. The second prototype is based on interconnecting two layers of HTS interconnects on separate substrates via solder bumps and flip chip techniques. Our development has centered around the HTS material $YBa_2Cu_3O_{7-\delta}$ (YBCO) which has a transition temperature of about 91 K (well above the boiling point of liquid nitrogen, 77 K) and critical current densities typically greater than 5 x 10^5 A/cm^2.

I. HTS MCM-D Prototype

A cross-section of our proposed HTS MCM is shown in Figure 1.

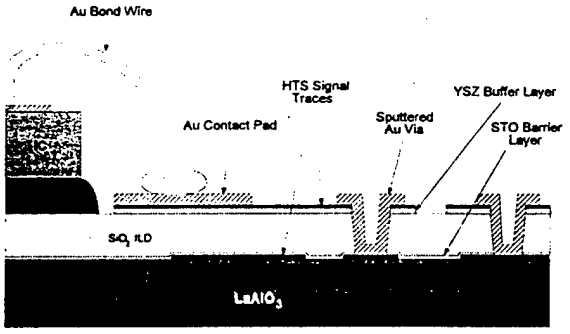

Figure 1. HTS MCM cross-section.

This novel structure has several key features that provide advantages over previously demonstrated HTS MCMs [2,3]. These advantages are:

(1) the utilization of an Interconnected Mesh Power System (IMPS) topology that is ideal for HTS multilayer fabrication because it allows an MCM to be constructed with only two layers of interconnects as opposed to the four that are traditionally used: x-signal, y-signal, and ground and power planes;

(2) a thick (~ 5 μm) layer of SiO_2 that is sandwiched between a thin buffer layer dielectric and a thin diffusion barrier layer dielectric to form a composite interlevel dielectric that is compatible with multilayer YBCO processing while allowing controlled impedance (Z_o = 50 Ω) lines to be fabricated, which are necessary for high speed signal propagation;

(3) chemical-mechanical polishing to create a planar SiO_2 surface for deposition of a high quality top level superconductor/buffer layer;

(4) high-aspect ratio, low contact resistance vias that utilize noble metals to form contacts between the two layers of YBCO interconnects, as opposed to large area, low-aspect ratio superconducting vias that have been fabricated with marginal success previously.

Due to the grain boundary problems associated with making very wide, sloping superconducting vias through a thick dielectric layer, alternative methods have to be explored to create the compact, high-aspect ratio vias necessary for fast, high density HTS MCMs.

Yttria stabilized zirconia (YSZ) was chosen as the material for providing a diffusion barrier/buffer layer between the superconductor and the interlevel dielectric material, silicon dioxide, because of its diffusion barrier properties as well as having a close lattice spacing and coefficient of thermal expansion (CTE) match to YBCO. Silicon dioxide was chosen as the interlevel dielectric material because of its low dielectric constant and well developed deposition and etching processes.

Experimental Details

Our MCM-D substrate was constructed of two layers of laser-ablated YBCO interconnects separated by a multilayer dielectric consisting of $SrTiO_3/SiO_2/YSZ$. We are able to attain critical current densities > 5 x 10^5 A/cm^2 in both YBCO layers. The laser-ablated $SrTiO_3$ (STO) and ion beam assisted laser-ablation deposited (IBAD) YSZ (yttria-stabilized zirconia) layers were ~0.5 μm thick while the reactively-sputtered SiO_2 ranges between 4 and 5 μm thick. The multilayered thin film structure is fabricated on 15 mm x 15 mm $LaAlO_3$ and YSZ substrates.

The HTS MCM was layed out as shown in Figure 2 on the following page.

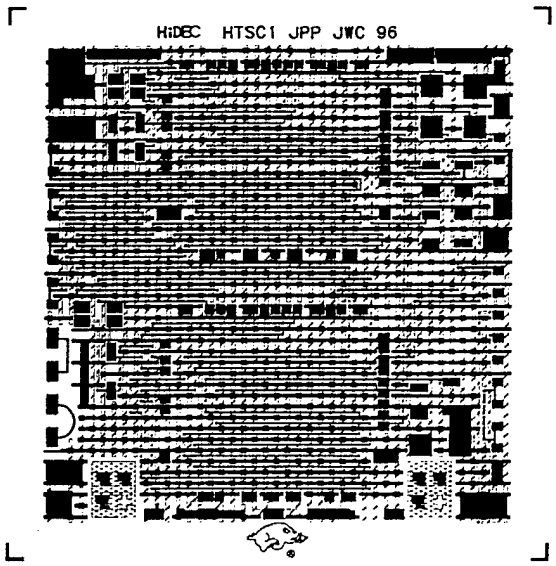

Figure 2. Layout of a 2 layer 15 mm x 15 mm HTS MCM-D substrate.

The 2.25 cm^2 substrate consists of two separate ring oscillators built using YBCO interconnects between two digital GaAs bare die (4.4 mm x 3.5 mm). The first ring oscillator is connected using the smallest possible interconnection, whereas, the second is connected by a much longer interconnect. A performance comparison between the two oscillators is planned for future work. There are also bond pads on the substrate for mounting various sizes of surface mount decoupling capacitors and terminating resistors. A prototype of our ring oscillator using one of the GaAs bare die wirebonded to 20 mil wide copper traces on a PC board was tested at liquid nitrogen temperature and was found to oscillate at ~250 MHz. Based on this result, our HTS MCM ring oscillator is estimated to operate at about the same frequency.

The via fabrication process is shown in Figure 3. The etching involves a 500 eV ion mill through the top YSZ buffer layer, which is followed by a reactive ion etch (RIE) through the SiO_2 interlevel dielectric selectively stopping at the barrier layer of STO. To complete the etching process, a 500 eV ion mill is done to etch through the STO and into the underlying YBCO. The final milling is very nonselective and requires close observation to keep from overetching through the bottom layer of YBCO. When depositing the top layer of YBCO at ~700° C, whatever material is deposited on the via sidewalls is presumably corroded due to interdiffusion of Si from SiO_2 into the YBCO but, presumably, does not affect the quality of the via. The subsequent *in situ* deposition of ~2000 Å of Au by laser ablation creates low resistance contacts without having to do a high temperature anneal in oxygen as was described by Ekin et al. [4]. This Au capping layer also acts as a passivation layer for the YBCO. In similar structures, contact resistivities of less than 10^{-7} Ω-cm^2 have consistently been attained. An additional 1.5-2.0 µm of Au is deposited over the existing YBCO/Au and then patterned using ion milling and photoresist as a mask.

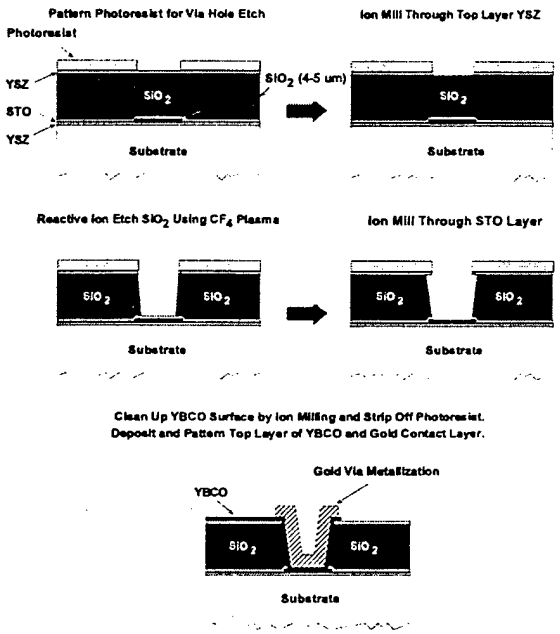

Figure 3. HTS via fabrication process.

This type of via structure has several advantages over previously demonstrated superconducting vias for use in HTS MCMs [2,3]. Since HTS thin films have to be deposited on planar surfaces or gradual slopes to maintain a reasonable current density, due to grain boundary problems, they require gradually sloped via holes that take up a wide area. By using a noble metal, compact, high-aspect ratio vias can be fabricated reliably.

Ultrasonic Al wire bonds were then made between YBCO/Au bond pads on the substrate and a wire bondable PC board. Via chain resistance was measured using a conventional 4-point contact configuration and measuring the voltage drop across the vias while passing DC current through it. The resistance vs. temperature of a ~0.5 cm long via chain structure with ten 40 µm square vias interconnecting 50 µm wide YBCO lines is shown in Figure 4. The room temperature resistance was measured to be about 515 Ω, and upon cooling to 78.5 K, the resistance dropped to about 87 Ω. As is shown in this figure, there are two separate superconducting transitions occurring at about 89 K and 80 K, which correspond to the top and bottom layer YBCO transitions. At 78.5 K, the interconnects had not yet become fully superconducting.

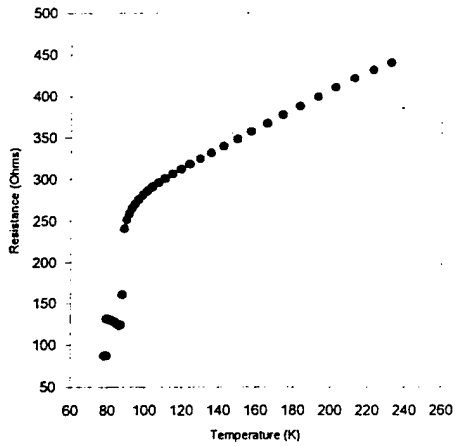

Figure 4. Temperature transition of a chain of ten 40 μm wide vias.

II. Flip-Mesh HTS MCM

The Flip-Mesh Superconducting Multi Chip Module (MCM) is an alternative to the conventional multi-layer superconducting MCM. It is desired that a superconducting MCM be fabricated using High-Temperature Superconductor (HTS) materials, with which such an MCM can be cooled using liquid nitrogen. However, many difficulties arise in the formation of multiple superconducting planes separated by dielectric layers on a single substrate. The crystalline nature of HTS materials such as Yttrium-Barium-Copper-Oxide (YBCO) requires that the deposition surface be closely matched to the HTS material in crystalline structure.

The high temperatures needed to form HTS materials requires that the other HTS MCM materials be matched with the superconductor in coefficient of thermal expansion (CTE), and not crack or delaminate at such high temperatures. These requirements lead to a complex stack of materials in order to create a multiple-superconducting-plane MCM interconnect structure. This combination of materials also complicates selective patterning processes with respect to the HTS material.

Flip-Mesh Basics

The fundamental concept of Flip-Mesh is that instead of depositing multiple HTS layers on a single substrate and connecting the layers by vias, single HTS layers are deposited on multiple substrates, and opposing superconducting layers on separate substrates are connected by flip-chip technology. This reduces the number of high-temperature processing steps to one, eliminating most of the difficulties in the multi-layer structure. However, the use of I/O technology to form vias limits the ultimate density of the Flip-Mesh Superconducting MCM.

In the multilayer MCM, Ion Beam Assisted Deposition (IBAD) [5] is used to form an oriented buffer layer so that an HTS film can be grown on an amorphous surface. This also allows the use of an amorphous substrate. Since Flip-Mesh requires only one superconducting plane per substrate, it is an ideal application for depositing HTS films on amorphous substrates. Amorphous substrates are considerably less costly than single-crystal substrates.

Flip-Mesh Substrate Arrangement

There are three substrates in a Flip-Mesh module. The main substrate contains *x*-plane interconnect and bonding sites for chips. Two smaller secondary substrates contain *y*-plane interconnect, and are "flipped" onto the main substrate. The chip bonding sites are between the secondary substrates. I/O pads are located on the outside edges of the main substrate. The Flip-Mesh substrate configuration is shown in Figure 5. As with the multilayer MCM, the Interconnected Mesh Power System (IMPS) topology [6] allows complete power, ground, and signals to be formed in two conducting planes. The term "Flip-Mesh" is derived from the flipping of IMPS-mesh interconnect planes to form an MCM interconnect structure.

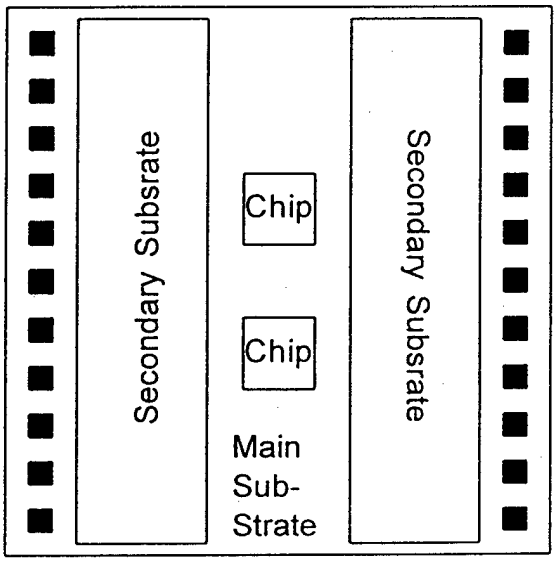

Figure 5. Flip-Mesh substrate configuration.

Flip-Mesh Substrate Processing

YBCO films are formed by laser ablation [7] on 1/2" or 1" square single-crystal yttria-stabilized zirconia (YSZ) or IBAD YSZ-buffered alumina substrates. The YBCO films are then patterned by argon ion milling [8] using conventional photoresist as a mask. The fact that ion milling is non-selective is not important in Flip-Mesh, since the underlying layer is always the substrate, which can be over-etched. The ion milling system is equipped with a water cooled sample stage to prevent YBCO or photoresist damage due to excessive heating from the ion milling.

Gold pads are then formed where electrical contact to YBCO is desired. A lift-off process is employed in which 2 μm of gold is sputter deposited onto a patterned photoresist layer. The Flip-Mesh substrates are exposed to a brief low-energy ion milling, which serves to prime the exposed YBCO surface for the gold deposition. After deposition, the photoresist layer is lifted off in an ultrasonic bath of acetone, leaving the gold pads on the YBCO. The lift-off process again avoids selective etching with respect to the YBCO. The Flip-Mesh substrates are then annealed at 600 °C for 1 hour in 500 Torr of oxygen to form a sturdy low-resistance contact.

The critical element of Flip-Mesh is the material used for the vias and the method used to form the interconnection. Figure 6 shows a cross-section of a Flip-Mesh via bump.

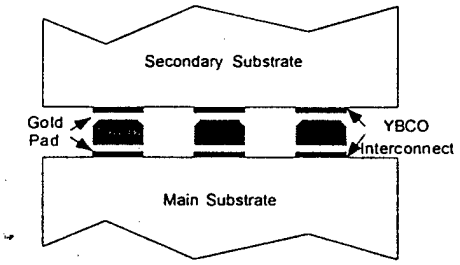

Figure 6. Flip-Mesh via cross-section.

The initial approach was to form gold balls using a ball bonding machine, and then press the substrates together while heating. Ball placement was found to be tedious, but workable. It was discovered, however, that the ball bonding process would often damage the underlying YBCO. This was not obvious unless the gold ball detached from the bonding pad. Ball detachment can be avoided by attaching to a bonding pad that is at least 1.5 times the size of the ball, but it is believed that this only disguises the damage.

Typical gold ball sizes range from 70 μm to 100 μm in diameter. The size of the Flip-Mesh bonding pad is 100 μm. Since density is already a limiting factor in the Flip-Mesh approach, increasing the via size is not desirable. It was also found that the extreme heat and pressure required to make an acceptable contact between the Flip-Mesh substrates caused the YBCO to become non-superconducting. The YBCO could be repaired by annealing, but the substrates would detach in the process.

The second assembly method attempted was to individually place preformed indium spheres. Indium was chosen because of its decent conductivity and low melting point. It was quickly discovered, however, that indium is far too soft to be handled mechanically, and no modules could be formed using this method. Stencil printing was then determined to be the ideal method for placing Flip-Mesh via bumps. A batch process would certainly be desirable, but the small via size (4 mil) and pitch (8 mil) puts severe limitations on this technology.

The first material to be screen printed was conductive epoxy, but this material was unable to meet the density requirement. The epoxy bumps would flatten and create shorts. Further work with the viscosity of the epoxy may lead to a useful application.

The next stencil printing material used was tin/lead solder. A special high-density solder was acquired, and worked nicely, but standard tin/lead solder has a leaching problem with the gold contact pads. Modules fabricated in this process detached within hours due to the leaching. Another solder paste was then acquired, which contained an additional 2% silver to prevent gold leaching.

After screen printing solder pads to the main substrate, the secondary substrates are aligned to the main substrate, and the solder is reflowed. The current Flip-Mesh material components are laser-ablated YBCO on single-crystal YSZ substrates with gold contact pads interconnected by screen printed tin/lead/silver solder bumps.

Initial Flip-Mesh Circuit

The initial Flip-Mesh circuit is a ring oscillator formed from 2 quad-XOR HCMOS chips. The first XOR gate has one input tied high, which turns it into an inverter. The other gates have one input tied low, which makes them buffers. This arrangement permits the number of gates in the loop to be adjusted from 2 to 8, allowing different speeds of oscillation.

The IMPS power and ground stripes are 250 μm wide, the signals are 50 μm wide, and the spacing between the two is 50 μm. The main substrate is 10

mm x 10 mm, and the secondary substrates are 2.5 mm x 10 mm. As was discussed previously, the contact pads are 100 μm x 100 μm. The XOR chips are approximately 1mm x 1mm each.

Flip-Mesh Assembly and Testing

After a Flip-Mesh substrate module is completed, the XOR chips are attached using thermoplastic tape. The leads of the chips are then aluminum wire bonded to the main substrate. The number of gates in the oscillator loop is selected by a wire bond in the center of the main substrate. The assembled Flip-Mesh module is then attached to a test board using thermoplastic tape. The I/O pads of the module are then aluminum wire bonded to the test board.

When complete, the test board is attached to an oscilloscope and power supply, measuring the output signal of the first XOR gate. The module is then slowly immersed in a small dewar of liquid nitrogen.

Conclusions

In summary, 40 μm YBCO/Au via chain structures have been characterized for use in an MCM-D substrate. The preliminary work shown here is to be improved upon by improving the quality of the YBCO layers, lowering the contact resistances, and possibly improving the step coverage of Au through the via by increasing its thickness. We are hoping to have an HTS MCM-D substrate fabricated in the near future. The performance of this MCM will be compared to that of a nearly identical Al interconnect module operating at liquid nitrogen temperature.

Thus far, functional Flip-Mesh modules have been fabricated only with metal interconnects. These modules were built on glass substrates with gold/titanium-tungsten metallization, and the substrates were interconnected with gold balls formed by a ball bonder. These units were tested both at room temperature and while immersed in liquid nitrogen with 2 to 8 gates in the oscillator loop. As would be expected, the modules ran faster at cryogenic temperature. While the gold ball vias worked adequately for a metal module, they were found to be incompatible with YBCO due to damage caused by the attachment process. The stencil printing processes discussed are under investigation to find a YBCO-compatible process. It will be interesting to compare the performance of the HTS Flip-Mesh to the cryogenic metal Flip-Mesh.

Despite the great processing complexity involved with fabricating an HTS MCM, great progress is being made toward achieving practical MCM substrates utilizing these novel materials.

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PRESENTATION: paper

FABRICATION AND CHARACTERIZATION OF A HIGH TEMPERATURE SUPERCONDUCTING MULTICHIP MODULE

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A process for fabricating high temperature superconducting (HTS) multichip module - deposited (MCM-D) substrates has been developed and tested. The module consists of two digital gallium arsenide bare die connected by $YBa_2Cu_3O_{7-\delta}$ (YBCO) HTS interconnects to form two ring oscillators on a 2.25 cm^2 MCM-D substrate. The interconnections consist of two wiring layers of YBCO separated by a 4-5 μm silicon dioxide interlevel dielectric. The 50 μm wide signal lines are routed between 150 μm power and ground lines with 75 μm spacings to form an interconnected mesh power system (IMPS). Connection between the two YBCO layers is accomplished with low contact resistance 40 μm gold vias through the interlevel dielectric layer. Ultrasonic Al wire bonds serve as electrical connections to gold/YBCO bond pads on the MCM substrate.

INTRODUCTION

One of the most promising applications for high temperature superconductors (HTSs) is as signal interconnects between integrated circuits (ICs) on multichip module (MCM) substrates. Unlike that of VLSI technologies where smaller feature sizes in successive generations allow interconnect lengths and power dissipation to be reduced, MCMs will not have that same luxury. As the complexity of ICs advances, both the pinout count per IC and the operating frequency will increase. However, MCM normal metal interconnections will be required to grow in length and will not be allowed to reduce in cross-sectional area. On MCM-D substrates, typical copper or aluminum interconnection dimensions are about 2 to 5 μm in thickness and between 15 and 30 μm wide. The resistivity of copper or aluminum decreases by at least a factor of 7 when decreasing the temperature from 300 K to 77 K (liquid nitrogen temperature), which allows smaller cross-section interconnects to be fabricated on cryogenically cooled MCMs. In order to increase the

wiring density in MCMs beyond that of cryo-cooled MCMs and improve the chip-to-chip bottleneck at high frequencies, alternatives to conventional metal interconnects must be considered [1].

HTS interconnections with negligible resistivity at operating frequencies of several tens of GHz and lower have great potential to reduce the interconnection line cross-section further with typical thicknesses being less than 1 μm and widths less than 2 μm for MCM applications. The critical current density of HTS interconnects, which limits the line's minimum cross-section, is similar in value to the maximum current density allowed in Al interconnects to inhibit electromigration. These small, low resistance interconnects offer significant performance advantages over normal metal interconnects for MCM-D technology using CMOS or GaAs integrated circuits which have enhanced chip level performance at liquid nitrogen temperatures (77 K). An added benefit of HTS lines is the reduced capacitive coupling between adjacent interconnections (due to their reduced thickness) which allows the lines to be spaced more closely together. The reduced cross-section of HTS interconnects should allow a significant increase in packing density and a corresponding decrease in the number of interconnect layers required to achieve the same functionality with normal metal interconnects.

HTS MCM DESCRIPTION

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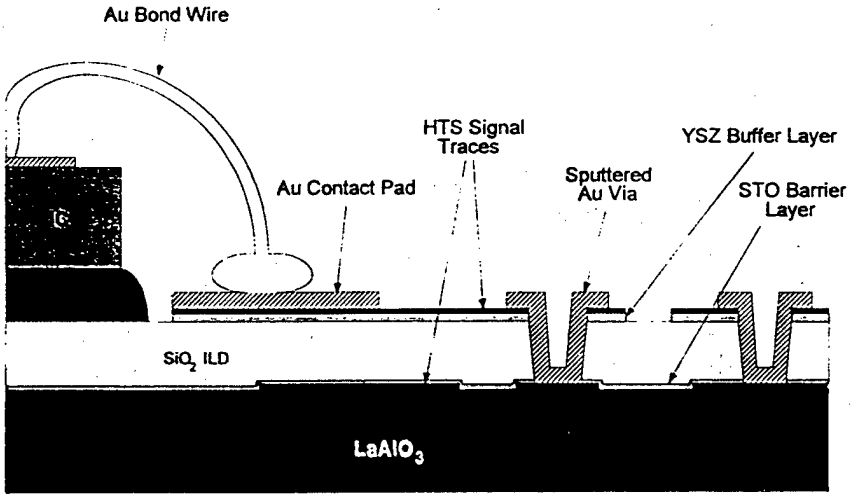

Figure 1: HTS MCM cross-section.

This novel structure has several key features that provide advantages over previously demonstrated HTS MCMs [2,3]. These advantages are:

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EXPERIMENTAL DETAILS AND RESULTS

The HTS MCM-D substrate was layed out as shown in Figure 2. The 2.25 cm^2 substrate consists of two separate ring oscillators built using YBCO interconnects to connect two digital GaAs bare die (4.4 mm x 3.5 mm). The first ring oscillator is connected using the shortest possible signal line, whereas the second is connected by a much longer interconnect. A performance comparison between the two oscillators is planned for future work. There are also bond pads on the substrate for mounting various size surface mount decoupling capacitors and terminating resistors. A prototype of our ring oscillator using one of the GaAs bare die wirebonded to 20 mil wide copper traces on a PC board was tested at liquid nitrogen temperature and was found to oscillate at ~250 MHz. Based on this result, our HTS MCM ring oscillator is estimated to operate at about the same frequency.

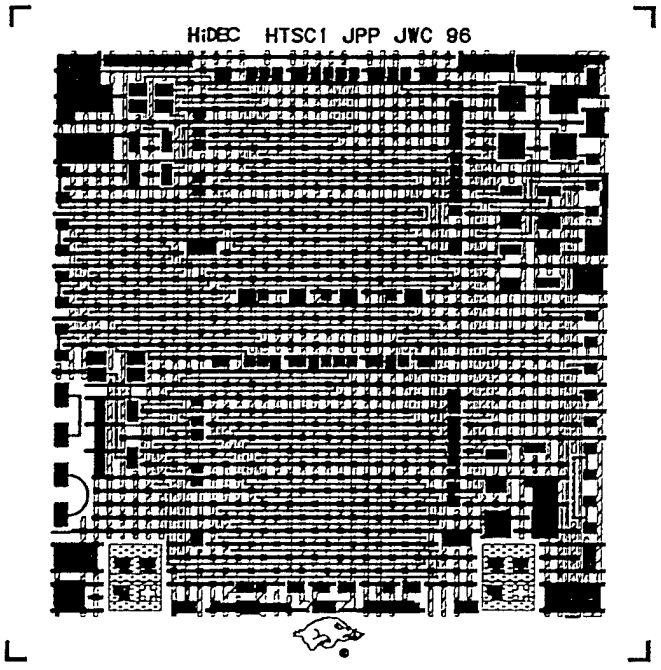

Figure 2: Layout of a 2 layer 15 mm x 15 mm HTS MCM-D substrate.

The HTS substrate was constructed of two layers of laser-ablated YBCO interconnects separated by a multilayer dielectric consisting of $SrTiO_3/SiO_2$/YSZ. The details of this technique will be described elsewhere [5]. The first layer of YBCO was deposited on a 15 mm x 15 mm single crystal substrate of $LaAlO_3$ or YSZ at a temperature of ~750° C to a thickness of 3000-3500 Å using a Lambda Physik LPX300 ArF excimer laser (λ = 193 nm) focused onto a rotating 1" diameter stoichiometric YBCO target. For thin film YBCO deposition, a pulse energy density of ~3-4 J/cm^2 at a 6 Hz repetition rate was used in a deposition chamber maintained at an oxygen pressure of 150-200 mTorr. We are able to attain critical current densities > 5 x 10^5 A/cm^2 in both YBCO layers. The YBCO was patterned using photolithography and 500 eV ion milling with a 30 mA beam current. The 3000-4000 Å thick $SrTiO_3$ (STO) diffusion barrier layer was laser-ablated at a pulse energy density of ~3-4 J/cm^2 with an 8 Hz repitition rate at a substrate temperature of ~650° C. The SiO_2 interlevel dielectric was deposited to a thickness of 4-5 μm by reactively sputtering a 3" diameter pure silicon target at an RF power of 180 W in a gas mixture of 83% argon/27% oxygen at a deposition pressure of 16 mTorr. The films were deposited at room temperature at a deposition rate of ~0.55 μm/hr.

After the SiO_2 deposition, the sharp step edges at the surface of the dielectric from nonconformal coating of the patterned bottom layer of YBCO must be smoothed out or planarized. This process is necessary to minimize the YBCO grain boundary dislocations

that would occur at 90° step edges and thereby to insure good quality layers of IBAD YSZ and YBCO are formed in the top interconnect layer [6]. To accomplish the SiO_2 step edge reduction, a chemical-mechanical polishing (CMP) process is performed using an alkaline (pH ~11) slurry consisting of ~100 nm silica particles in a mixture of potassium hydroxide and DI water [7]. The solution is dispersed onto a Rodel IC1000 porous, urethane polishing pad spinning at a rate of 50 rpm. The samples are mounted to a holder and rotated at a rate of 65-70 rpm opposite the direction of the polishing pad. Polishing at a force of 10 lb for 3 minutes results in a reduction of a 935 nm tall spike and a sharp 284 nm step edge to a 27 nm hump as shown in Figure 3.

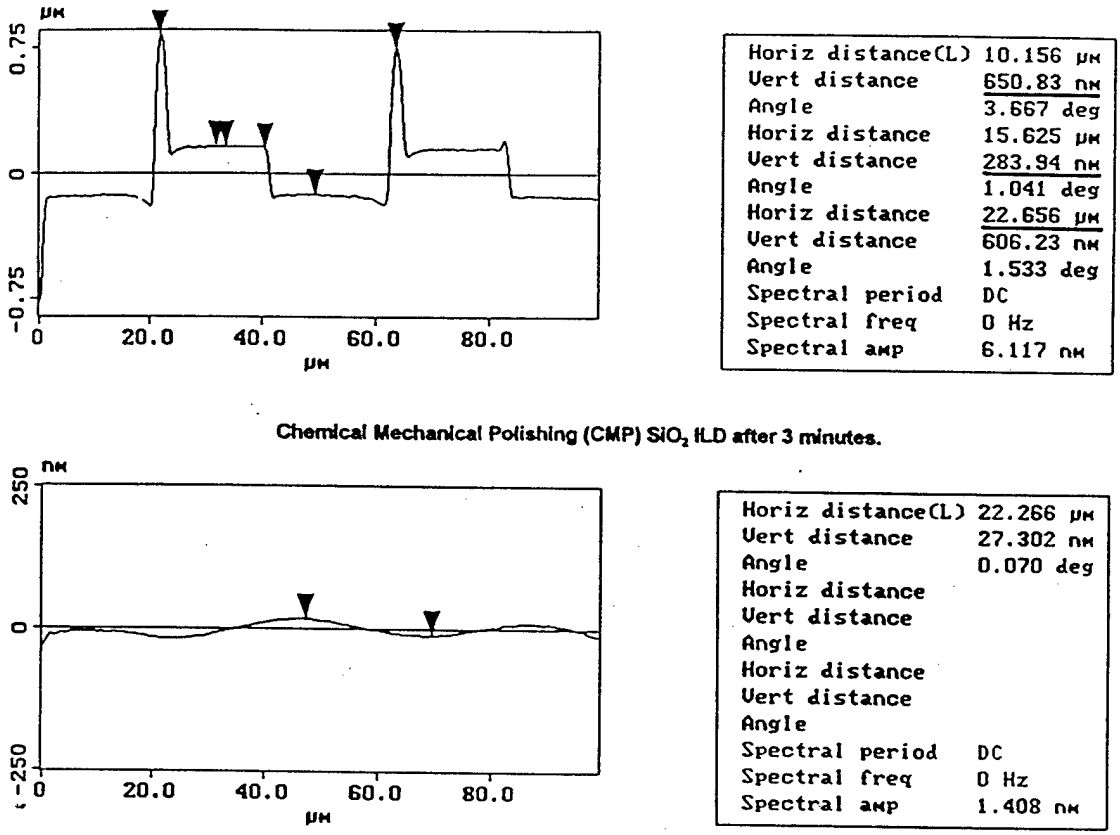

Figure 3. Step height reduction using silicon dioxide chemical-mechanical polishing (CMP) process.

Following planarization and cleanup, a layer of YSZ was deposited using an ion beam assisted deposition (IBAD) technique along with laser-ablation to attain a textured film at room temperature [8]. Briefly, the technique involves positioning an ion gun at a distance of ~14 cm from the substrate and at an angle of 55° from the substrate normal. Argon gas is flowed through the ion gun at a rate of 20 sccm and directed at the sample at a beam

energy of 250 eV and beam current of 15 mA while the laser deposition is occuring. The final thickness of the YSZ film was ~3000-4000 Å.

The via fabrication process is shown in Figure 4.

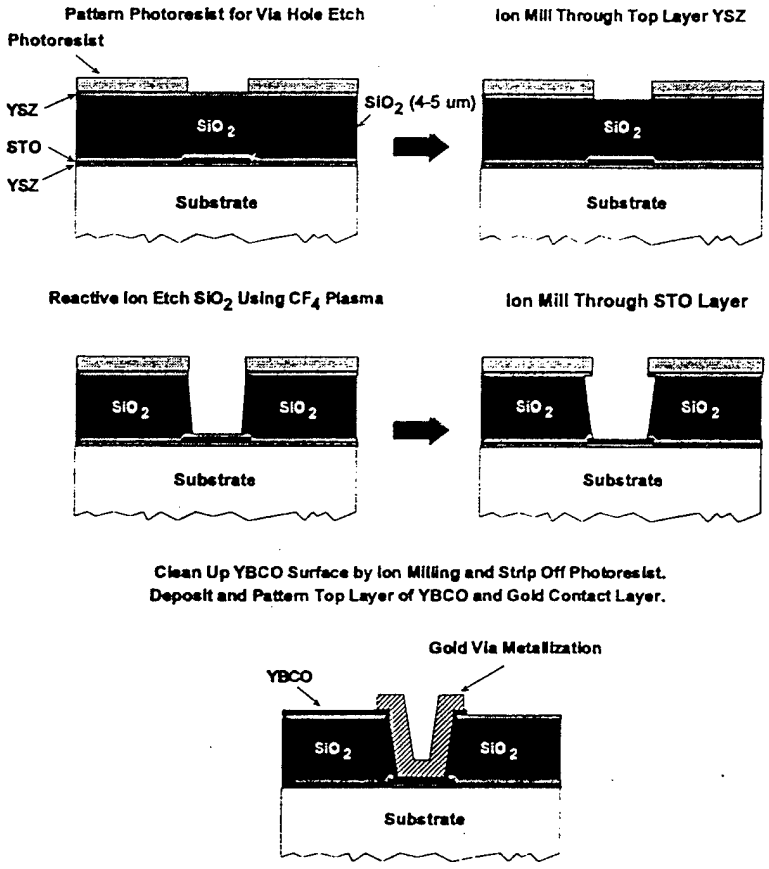

Figure 4: HTS via fabrication process.

The etching involves a 500 eV ion mill with a beam current of 30 mA through the top YSZ buffer layer, which is followed by a reactive ion etch (RIE) using a gas mixture of 85% CF_4/15% O_2 through the SiO_2 interlevel dielectric selectively stopping at the barrier layer of STO. To complete the etching process, a 500 eV ion mill at a beam current of 30 mA is done to etch through the STO and into the underlying YBCO. The final milling is very nonselective and requires close observation to keep from etching through the bottom layer of YBCO. When depositing the top layer of YBCO at ~700° C, whatever material is deposited on the via sidewalls is presumably corroded due to interdiffusion of Si from SiO_2 into the YBCO [9] but, presumably, does not affect the quality of the via. The subsequent *in situ* deposition of ~2000 Å of Au by laser ablation creates low resistance contacts without having to do a high temperature anneal in oxygen as was described by Ekin et al. [10]. This

Au capping layer also acts as a passivation layer for the YBCO. In similar structures, contact resistivities of less than 10^{-7} Ω-cm^2 have consistently been attained. An additional 1.5-2.0 μm of Au is deposited over the existing YBCO/Au and then patterned using ion milling and photoresist as a mask. This type of via structure has several advantages over previously demonstrated superconducting vias for use in HTS MCMs [2,3]. Since HTS thin films have to be deposited on planar surfaces or gradual slopes to maintain a reasonable current density, due to grain boundary problems, they require gradually sloped via holes that take up a wide area. By using a noble metal, compact, high-aspect ratio vias can be fabricated reliably. The additional resistance in the vias (series resistance and contact resistance) will be very small and will not give rise to unwanted RC delay provided there are not an excessive number of vias in the signal path.

Ultrasonic Al wire bonds were then made between YBCO/Au bond pads on the substrate and a wire bondable PC board. The via chain resistance was measured using a conventional 4-point contact configuration by measuring the voltage drop across the vias while passing DC current through it. The resistance vs. temperature of a ~0.5 cm long via chain structure with ten 40 μm square vias interconnecting 50 μm wide YBCO lines is shown in Figure 5. The room temperature resistance was measured to be about 515 Ω, and upon cooling to 78.5 K, the resistance dropped to about 87 Ω. As shown in this figure, there are two separate superconducting transitions occurring at about 89 K and 80 K which correspond to the top and bottom layer YBCO transitions. At 78.5 K, the interconnects had not yet become fully superconducting.

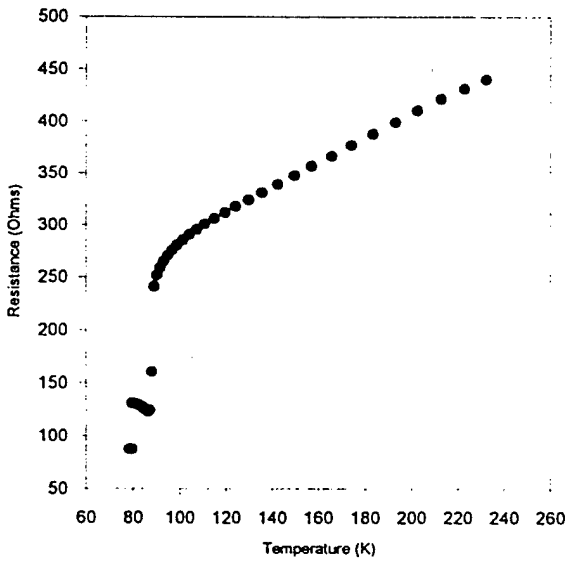

Figure 5: Temperature transition of a chain of ten 40 μm wide vias.

CONCLUSIONS

In summary, 40 μm YBCO/Au via chain structures have been characterized for use in an MCM-D substrate. The preliminary work shown here is to be improved upon by improving the quality of the YBCO layers, lowering the contact resistances, and possibly improving the step coverage of Au through the via by increasing its thickness. We are hoping to have an HTS MCM-D substrate fabricated in the near future. The performance of this MCM will be compared to that of a nearly identical Al interconnect module operating at liquid nitrogen temperature.

Despite the processing complexity involved with fabricating an HTS MCM, great progress is being made toward achieving practical MCM substrates utilizing these novel materials.

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CALL FOR PAPERS

FOURTH SYMPOSIUM ON LOW TEMPERATURE ELECTRONICS AND HIGH TEMPERATURE SUPERCONDUCTIVITY

191st Electrochemical Society Meeting, Montreal, Canada, May 4- 9, 1997

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PRESENTATION: Paper

THE FLIP-MESH SUPERCONDUCTING MCM

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One of the many possible applications of high-temperature superconducting (HTS) thin films is as interconnect in a hybrid multi-chip module (MCM). Such a module would consist of a substrate containing superconducting interconnect and conventional CMOS circuitry chips. Since HTS thin films are crystalline in nature and deposited at high temperatures, many difficulties arise in the formation of epitaxial multi-layer superconducting structures. The Flip-Mesh Superconducting MCM provides an alternative to a multi-layer substrate by interfacing multiple single-layer substrates, thereby reducing the epitaxy requirement to one layer per substrate. This substrate interfacing is accomplished by forming X-plane interconnect on one substrate and Y-plane interconnect on another, and connecting them using I/O technology. The reduced epitaxy requirement of Flip-Mesh also makes the implementation of amorphous substrates more feasible. The Interconnected Mesh Power System (IMPS) topology used so that power, ground, and signals can be fabricated on two planes.

FLIP-MESH BASICS

The Flip-Mesh Superconducting MCM is an alternative to the conventional multi-layer superconducting MCM. It is desired that a superconducting MCM be fabricated using HTS materials, with which such an MCM can be cooled using liquid nitrogen. However, many difficulties arise in the formation of multiple superconducting planes separated by dielectric layers on a single substrate. The crystalline nature of HTS materials such as yttrium-barium-copper-oxide (YBCO) requires that the deposition surface be closely matched to the HTS material in crystalline structure.

The high temperatures needed to form HTS materials requires that the other HTS MCM materials be matched with the superconductor in coefficient of thermal expansion (CTE), and not crack or delaminate at such high temperatures. These requirements lead to a complex stack of materials in order to create a multiple-superconducting-plane MCM interconnect structure. This combination of materials also complicates selective patterning processes with respect to the HTS material.

The fundamental concept of Flip-Mesh is that instead of depositing multiple HTS layers on a single substrate and connecting the layers by vias, single HTS layers are deposited on multiple substrates, and opposing superconducting layers on the separate substrates are connected by flip-chip technology. This reduces the number of high-temperature processing steps to one, eliminating most of the difficulties in the multi-layer structure. However, the use of I/O technology to form vias limits the ultimate density of the Flip-Mesh Superconducting MCM.

In the multilayer MCM, ion beam assisted deposition (IBAD) [1] is used to form an oriented buffer layer so that an HTS film can be grown on an amorphous surface. This also allows the use of an amorphous substrate. Since Flip-Mesh requires only one superconducting plane per substrate, it is an ideal application for depositing HTS films on amorphous substrates. Amorphous substrates are considerably less costly than single-crystal substrates.

FLIP-MESH SUBSTRATE ARRANGEMENT

There are three substrates in a Flip-Mesh module. The main substrate contains *x*-plane interconnect and bonding sites for chips. Two smaller secondary substrates contain *y*-plane interconnect, and are "flipped" onto the main substrate. The chip bonding sites are between the secondary substrates. I/O pads are located on the outside edges of the main substrate. The Flip-Mesh substrate configuration is shown in Figure 1. As with the multilayer MCM, the IMPS topology [2] allows complete power, ground, and signals to be formed in two conducting planes. The term "Flip-Mesh" is derived from the flipping of IMPS-mesh interconnect planes to form an MCM interconnect structure.

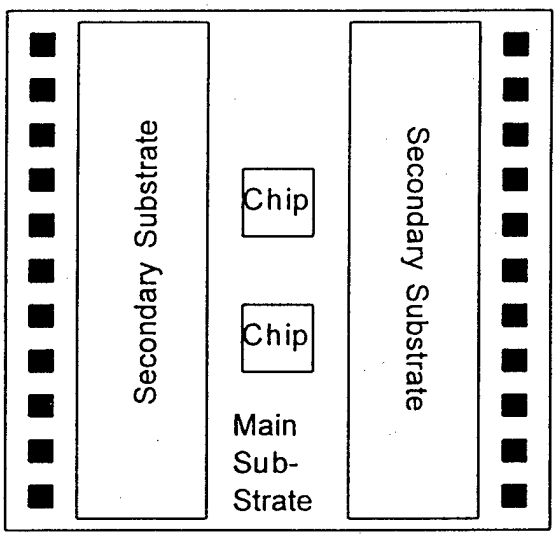

Figure 1: Flip-Mesh Substrate Configuration

FLIP-MESH SUBSTRATE PROCESSING

YBCO films are formed by laser ablation [3] on 1/2" or 1" square single-crystal yttria-stabilized zirconia (YSZ) or IBAD YSZ-buffered alumina substrates. The YBCO films are then patterned by argon ion milling [4] using conventional photoresist as a mask. The fact that ion milling is non-selective is not important in Flip-Mesh, since the underlying layer is always the substrate, which can be over-etched. The ion milling system is equipped with a water cooled sample stage to prevent YBCO or photoresist damage due to excessive heating from the ion milling.

Gold pads are then formed where electrical contact to YBCO is desired. A lift-off process is employed, where 2 μm of gold is sputter deposited on a patterned photoresist layer. The Flip-Mesh substrates are exposed to a brief low-energy ion milling, which serves to prime the exposed YBCO surface for the gold deposition. After deposition, the photoresist layer is lifted off in an ultrasonic bath of acetone, leaving the gold pads on YBCO. The lift-off process again avoids selective etching with respect to YBCO. The Flip-Mesh substrates are then annealed at 600 °C for 1 hour in 500 torr of oxygen to form a sturdy low-resistance contact.

The critical element of Flip-Mesh is the material used for the vias and the method used to form the interconnection. Figure 2 shows a cross-section of Flip-Mesh via bumps.

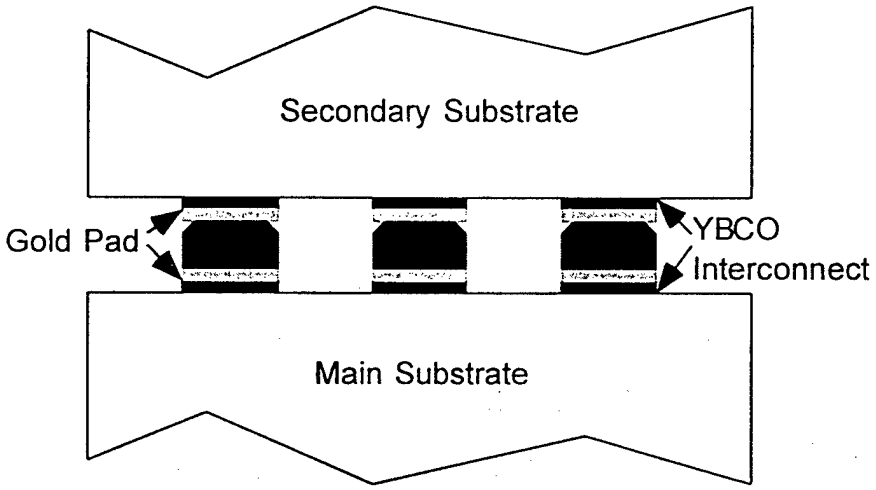

Figure 2: Flip-Mesh Via Cross-Section

The initial approach was to form gold balls using a ball bonding machine, and then press the substrates together while heating. Ball placement was found to be tedious, but workable. It was discovered, however, that the ball bonding process would often damage the underlying YBCO. This was not obvious unless the gold ball detached from

the bonding pad. Ball detachment can be avoided by attaching to a bonding pad that is at least 1.5 times the size of the ball, but it is believed that this only disguises the damage.

Typical gold ball sizes range from 70 μm to 100 μm in diameter. The size of the Flip-Mesh bonding pad is 100 μm. Since density is already a limiting factor in the Flip-Mesh approach, increasing the via size is not desirable. It was also found that the extreme heat and pressure required to make an acceptable contact between the Flip-Mesh substrates caused the YBCO to become non-superconducting. The YBCO could be repaired by annealing, but the substrates would detach in the process.

The second assembly method attempted was to individually place preformed indium spheres. Indium was chosen because of its decent conductivity and low melting point. It was quickly discovered, however, that indium is far too soft to be handled mechanically, and no modules could be formed using this method. Stencil printing was then determined to be the ideal method for placing Flip-Mesh via bumps. A batch process would certainly be desirable, but the small via size (4 mil) and pitch (8 mil) puts severe limitations on this technology.

The first material to be screen printed was conductive epoxy, but this material was unable to meet the density requirement. The epoxy bumps would flatten and create shorts. Further work with the viscosity of the epoxy may lead to a useful application.

The next stencil printing material used was tin/lead solder. A special high-density solder was acquired, and worked nicely, but standard tin/lead solder has a leaching problem with the gold contact pads. Modules fabricated in this process detached within hours due to the leaching. Another solder paste was then acquired, which contained an additional 2% silver to prevent gold leaching.

After screen printing solder pads to the main substrate, the secondary substrates are aligned to the main substrate, and the solder is reflowed. The current Flip-Mesh material components are laser-ablated YBCO on single-crystal YSZ substrates with gold contact pads interconnected by screen printed tin/lead/silver solder bumps.

INITIAL FLIP-MESH CIRCUIT

The initial Flip-Mesh circuit is a ring oscillator formed from 2 quad-XOR HCMOS chips. The first XOR gate has one input tied high, which turns it into an inverter. The other gates have one input tied low, which makes them buffers. This arrangement allows the number of gates in the loop to be adjusted from 2 to 8, allowing different speeds of oscillation. The IMPS power and ground stripes are 250 μm wide, the signals are 50 μm wide, and the spacing between the two is 50 μm. The main substrate is 10 mm x 10 mm, and the secondary substrates are 2.5 mm x 10 mm. As was discussed

before, the contact pads are 100 μm x 100 μm. The XOR chips are approximately 1mm x 1mm each.

FLIP-MESH ASSEMBLY AND TESTING

After a Flip-Mesh substrate module is completed, the XOR chips are attached using thermoplastic tape. The leads of the chips are then aluminum wire bonded to the main substrate. The number of gates in the oscillator loop is selected by a wire bond in the center of the main substrate. The assembled Flip-Mesh module is then attached to a test board using thermoplastic tape. The I/O pads of the module are then aluminum wire bonded to the test board. Figure 3 shows an assembled Flip-Mesh module connected to a test board. When complete, the test board is attached to an oscilloscope and power supply, measuring the output signal of the first XOR gate. The module is then slowly immersed in a small dewar of liquid nitrogen.

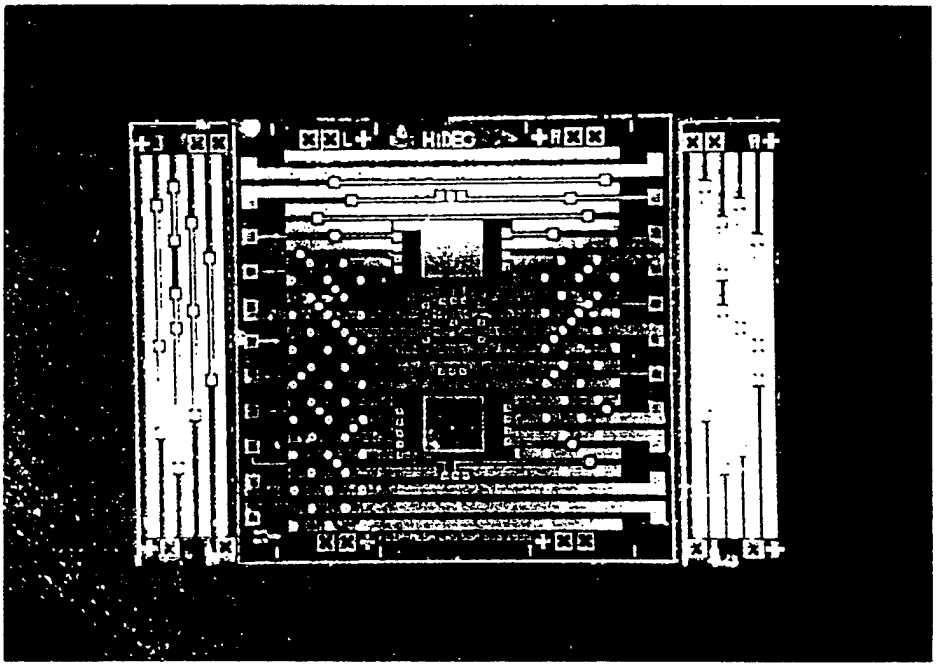

Figure 3: Assembled Flip-Mesh Module

CONCLUSION

Functional Flip-Mesh modules have been fabricated only with metal interconnect. These modules were built on glass substrates with gold/titanium-tungsten metallization, and the substrates were interconnected with gold balls formed by a ball bonder. These modules were tested both at room temperature and while immersed in liquid nitrogen with 2 to 8 gates in the oscillator loop. As would be expected, the modules ran faster at

cryogenic temperature. While the gold ball vias worked adequately for a metal module, they were found to be incompatible with YBCO due to damage caused by the attachment process. The stencil printing processes discussed are under investigation to find a YBCO-compatible process. It will be interesting to compare the performance of the cryogenic YBCO Flip-Mesh to the cryogenic metal Flip-Mesh.

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